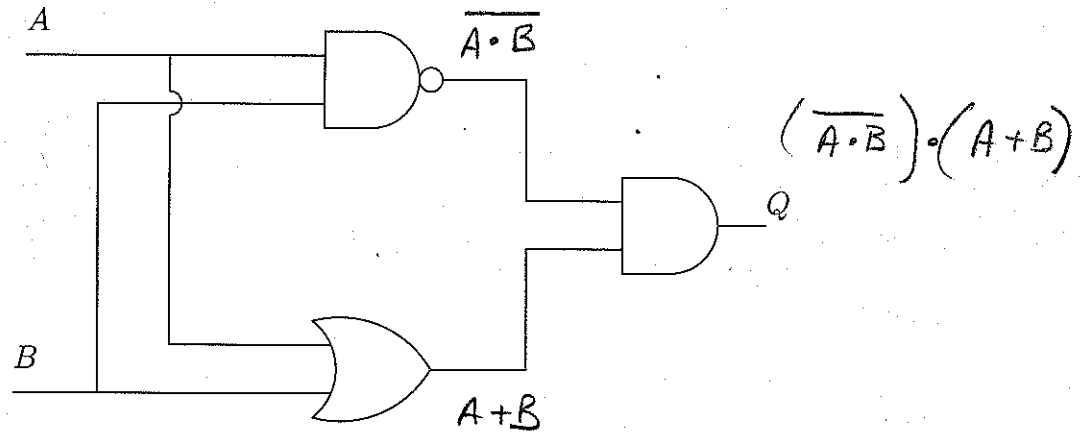


PHYS 235 — Exam #3
 Thursday, April 16, 2009

Name: _____

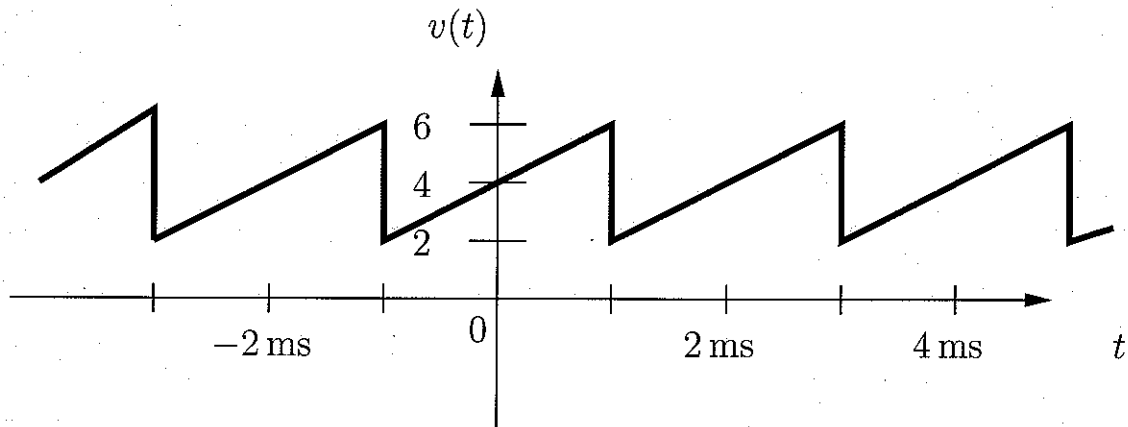
1. Determine the truth table for the illustrated combination of logic gates.



A	B	$A \cdot B$	$\overline{A \cdot B}$	$A + B$	$(\overline{A \cdot B}) \cdot (A + B)$
0	0	0	1	0	0
1	0	0	1	1	1
0	1	0	1	1	1
1	1	1	0	1	0

↑
 This is an XOR

2. Consider the following graph of a periodic voltage signal:



All (well-behaved) periodic signals can be represented by a Fourier series:

$$v(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos n\omega t + \sum_{m=1}^{\infty} b_m \sin m\omega t.$$

- Determine a quantitative value for a_0 .
- Determine a quantitative value for a_1 .
- Determine a quantitative value for b_1 .

a) $\frac{a_0}{2}$ is the average value of the function over 1 period, so $\frac{a_0}{2} = 4$ or $a_0 = 8$

b) Function is an offset odd function, so $a_n = 0$ for all $n > 1$

c) $T = 2 \text{ ms} \Rightarrow \omega = \frac{2\pi}{2 \text{ ms}} = \pi \text{ ms}^{-1} = 1000\pi \text{ s}^{-1}$

$v(t) = 4 + 2t$, where t in ms

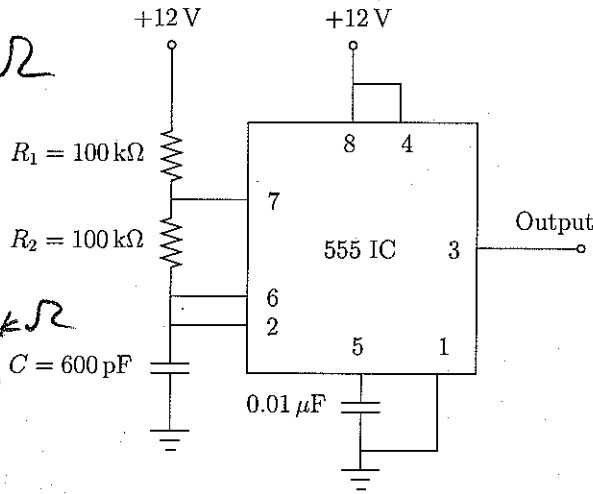
$$b_1 = \frac{2}{2} \int_{-1}^1 (4 + 2t) \sin \pi t \, dt = \frac{4}{\pi} \quad \leftarrow \text{ms}$$

$$\text{or } b_1 = \frac{2}{0.002} \int_{-0.001}^{0.001} (4 + 2000t) \sin 1000\pi t \, dt = \frac{4}{\pi} \quad \leftarrow \text{s}$$

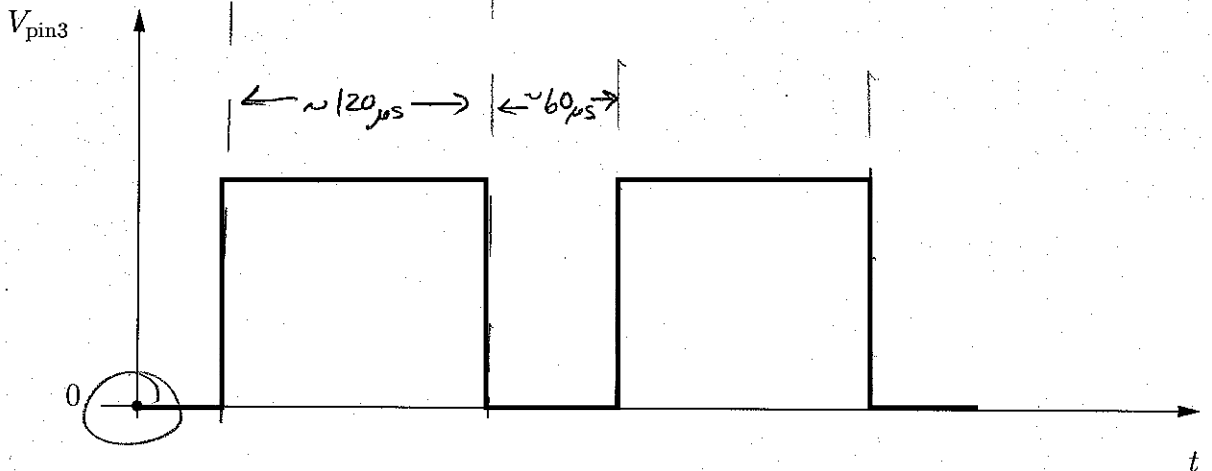
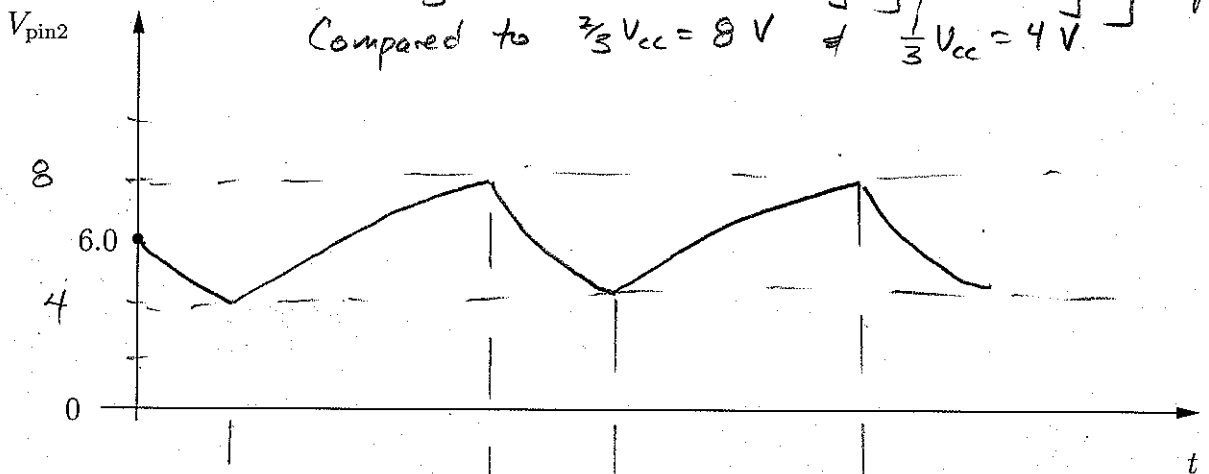
3. Sketch the indicated voltages for the illustrated circuit; include a time scale on your sketches. NOTE: Initial values are indicated on the graphs.

Charges through $200\text{ k}\Omega$
 $(RC)_{\text{charging}} = 2 \times 10^5 \times 6 \times 10^{-10}$
 $= 120\ \mu\text{s}$

Discharges through $100\text{ k}\Omega$
 $(RC)_{\text{discharge}} = 10^5 \times 6 \times 10^{-10}$
 $= 60\ \mu\text{s}$

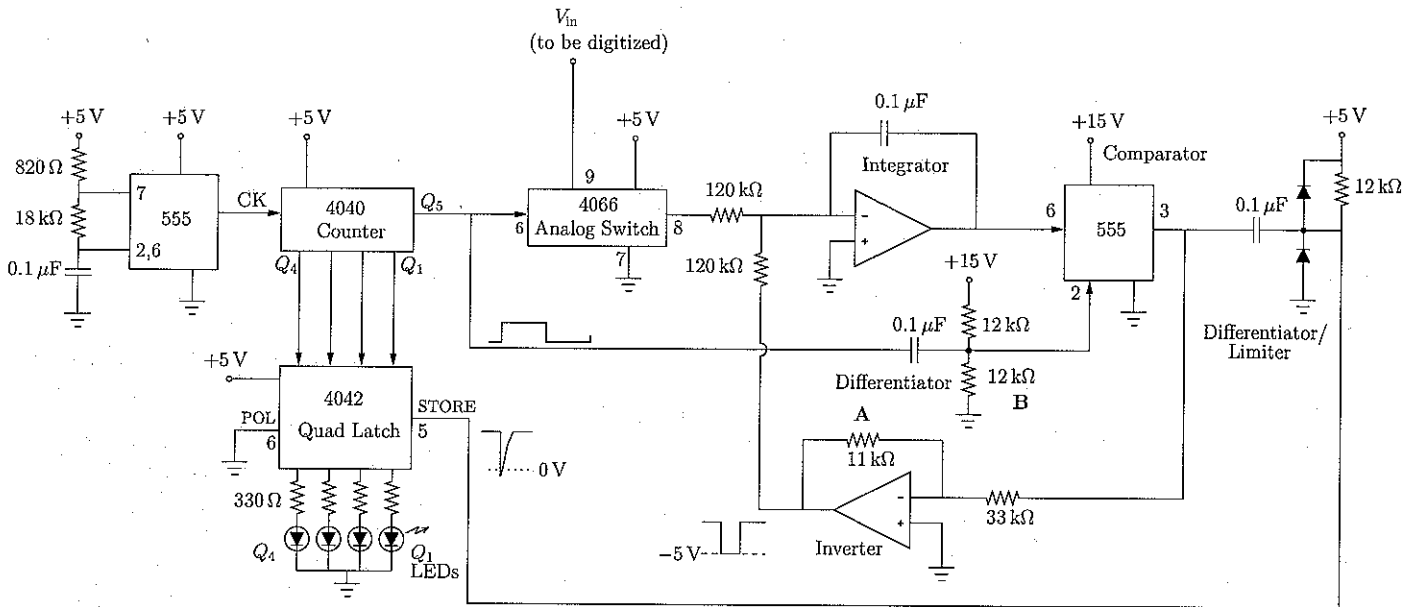


Voltage across a charging/discharging capacitor.
 Compared to $\frac{2}{3}V_{cc} = 8\text{ V}$ and $\frac{1}{3}V_{cc} = 4\text{ V}$.



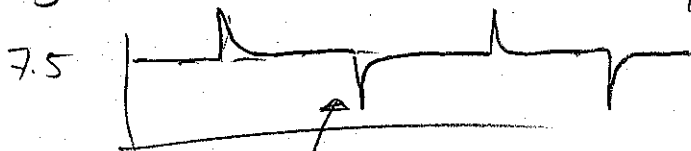
Output initially low
 $\Rightarrow Q1$ initially ON
 \Rightarrow Capacitor initially discharging.

4. In class you built the illustrated dual slope A-to-D converter. On the following page is the timing diagram that I recorded with an input voltage of 1.5 V.



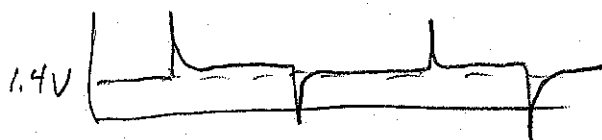
- (a) What is the binary output for the 1.5 V input? 0100_2
- (b) Redraw the timing diagram for an input voltage of 3.0 V. (If a given line is unchanged, simply say so.) *Changes integrator slope for downward portion.*
- (c) Imagine returning to the original input of 1.5 V, and then changing the indicated resistor at point A from its original value of 11 kΩ to 22 kΩ. Complete the new timing diagram. (If a given line is unchanged, simply say so.) *Changes inverter output, so changes integrator output during upward integration*
- (d) (Unrelated to previous parts.) You mistakenly use a 1.2 kΩ resistor at point B instead of a 12 kΩ resistor. Will your A/D converter still work? Explain.

Regular circuit: Pin 2 of comparator "sees"



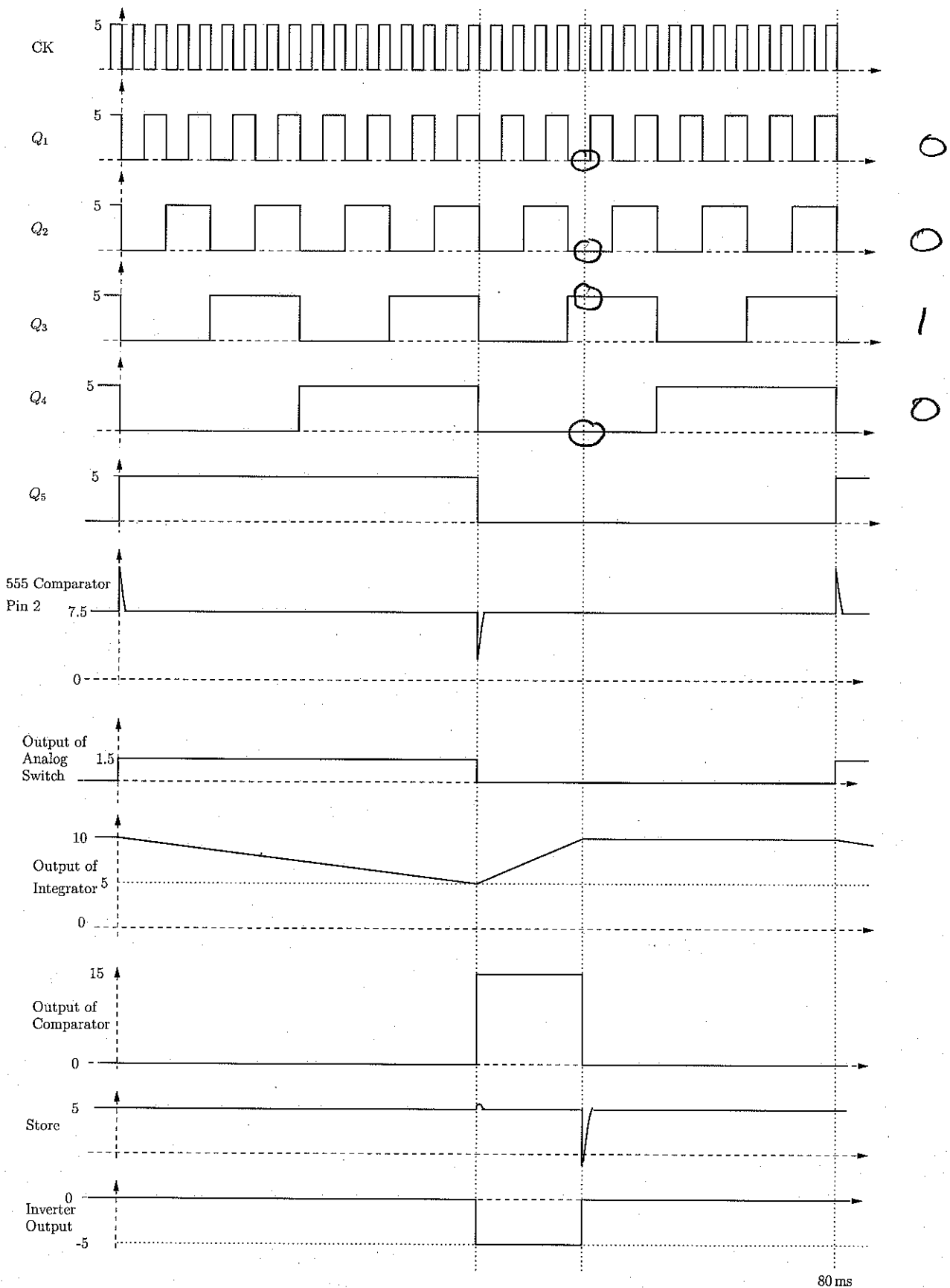
When pin 2 goes below 5V, comparator sets output high.

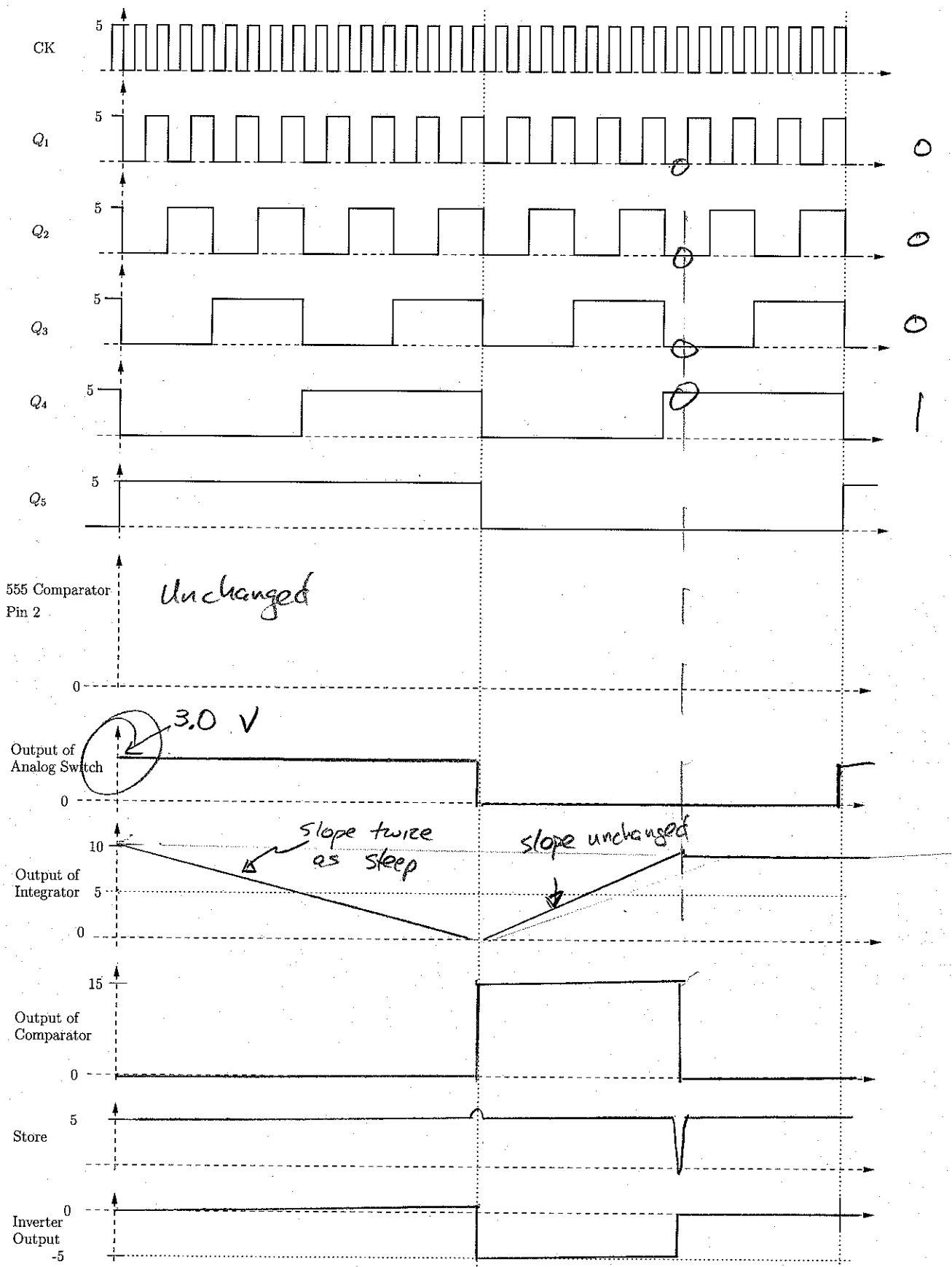
Modified circuit:



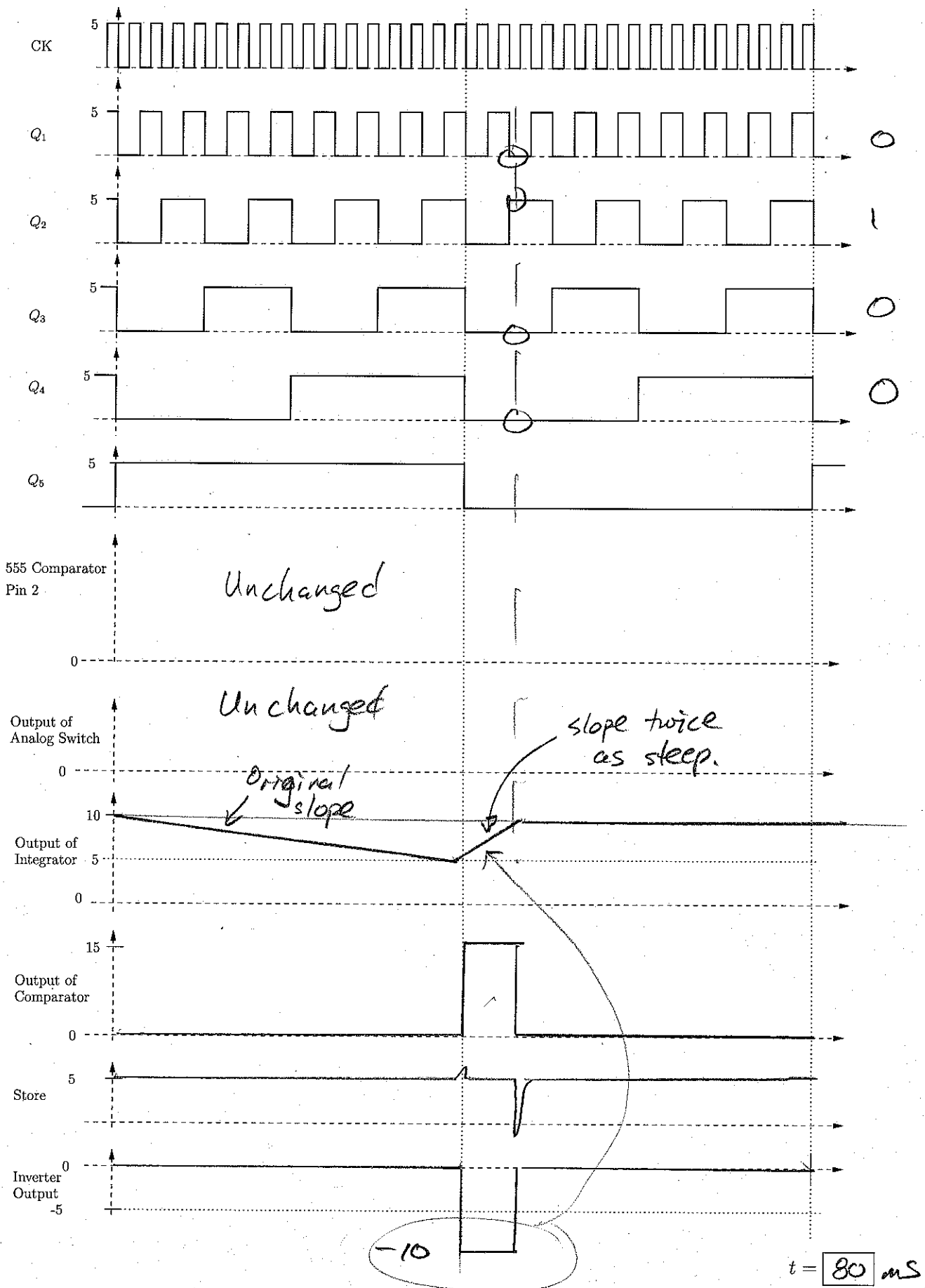
$$\frac{1.2 \text{ k}\Omega}{1.2 \text{ k}\Omega + 12 \text{ k}\Omega} \times 15 = 1.36 \text{ V}$$

Pin 2 always below 5. Circuit won't work

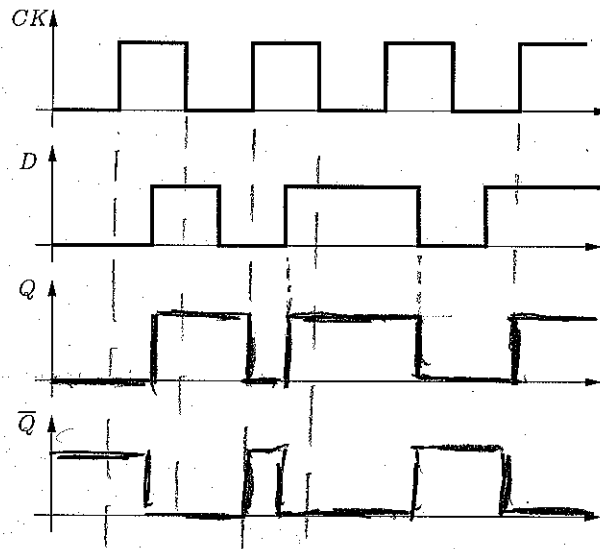
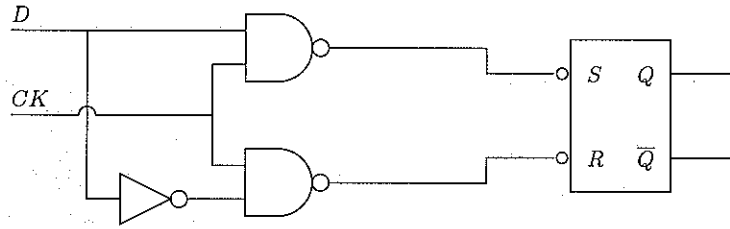




$t = 80 \text{ ms}$



5. (a) Write the truth table for the illustrated circuit.
 (b) Complete the timing diagram.



CK	D	\bar{D}	$\overline{D \cdot C}$	$\overline{\bar{D} \cdot C}$	Q	\bar{Q}
0	0	1	1	0	N.C. (hold input)	
0	1	0	1	1		
1	0	1	1	0	0	1
1	1	0	0	1	1	0

Inputs to an active-low flip-flop

Level-triggered flip-flop; Passes D to Q when ck high