PHYS 235: Homework Problems

78. Convert the following binary number to decimal:

$$(10110)_2 = (\_\_\_\_\_)_{10}$$

79. Convert the following decimal number to binary:

$$(49)_{10} = (\_\_\_\_\_)_2$$

80. Convert the following decimal number to hexadecimal:

$$(49)_{10} = (\_\_\_\_\_)_{16}$$

81. Convert the following hexadecimal number (base 16) to decimal:

$$(3F2)_{16} = (\_\_\_\_\_)_{10}$$

82. Convert the following decimal number to binary coded decimal (BCD):

$$(63)_{10} = (\_\_\_\_\_)_{\text{BCD}}$$

83. Convert the following binary coded decimal (BCD) number to decimal:

$$(1001\,0111)_{\text{BCD}} = (\_\_\_\_\_)_{10}$$

84. Write the truth tables for the following functions of two binary variables, and sketch the standard gate symbol. (You should be able to do this without looking them up.)

    (a) AND

    (b) NAND

    (c) OR

    (d) NOR

    (e) XOR

    (f) XNOR

85. Draw a schematic diagram showing how you would implement the following functions using only NAND gates.

    (a) $F = \overline{A}$

    (b) $F = A + B$

    (c) $F = A \cdot B$

    (d) $F = A \cdot \overline{B} + \overline{A} \cdot B$

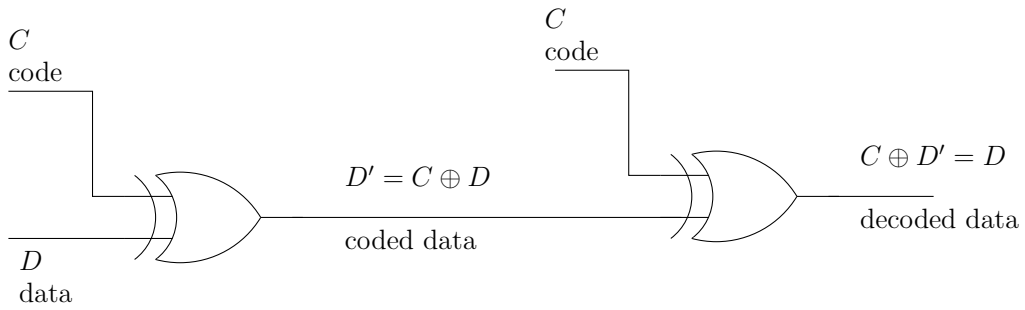
86. An XOR gate can be used to encode and decode data. Let's work through a simple example.

    (a) The ASCII code (American Standard Code for Information Interchange) is a common case-sensitive *alphanumeric* code that represents letters as numbers. Find an ASCII table and translate the the word "Hi" into a decimal number and a binary number:

    $$\text{Hi} \longrightarrow (\_\_\_\_\_)_{10} = (\_\_\_\_\_)_2$$

    (b) Imagine that the binary ASCII code for "Hi" is translated into a string of pulses that are fed to the data input in the circuit below. At the same time a string of coding pulses are fed to the C input. Determine the binary number that represents the coded data D' if the code is 01110100110111.

    (c) Verify that the second XOR gate returns the original message.



87. Design a flip-flop (latch) using cross-coupled NOR gates instead of the cross-coupled NAND gates you used in lab. (You should be able to do this without using any "external" resources, but if you get stuck you can look this up in your text or on-line.) Give the truth table for your flip-flop. Should your inputs be labeled (S, R), or ($\overline{S}$, $\overline{R}$)?

88. (a) Show that the operation of an XOR gate ($A \oplus B$) can be written as

$$A \oplus B = A \cdot \overline{B} + \overline{A} \cdot B.$$

(b) Based on this identity, draw a circuit diagram showing how to realize an XOR gate using only NAND gates.

89. (a) Show that the operation of an XOR gate ($A \oplus B$) can be written as

$$A \oplus B = (A + B) \cdot (\overline{A \cdot B})$$

(b) Based on this identity, draw a circuit diagram showing how to realize an XOR gate using only NAND gates. (This should be a different circuit than the one drawn for the previous problem).

90. Table 8.3 on p. 209 of Eggleston, (or Table 12.8 on p. 540 of Simpson, or ...) gives several Properties of Boolean Operations. By examining the truth tables for the AND and the OR gates you should be able to convince yourself that *all* of these relationships are true. Specifically, give arguments that demonstrate that

(a) $A + \overline{A} = 1$, and

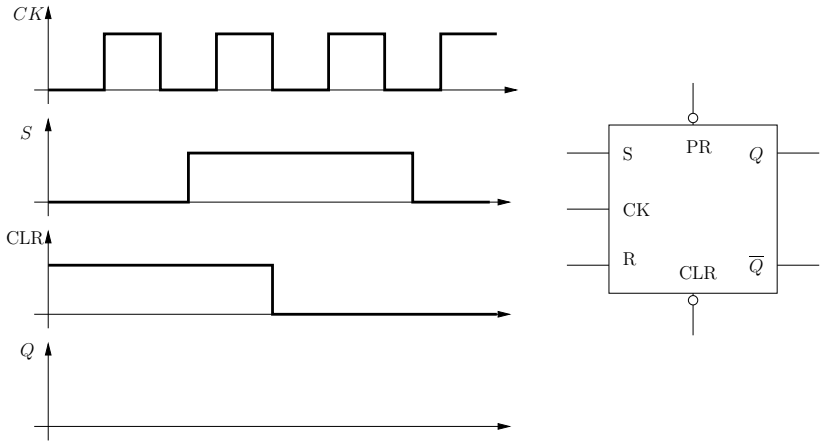
(b) $A \cdot A = A$.

91. There are many commutative, distributive, and associative rules for Boolean operations. **NOTE:** In Boolean expressions there are often some suppressed parentheses and implied order of operations, just like there are for normal addition and multiplication. For example $A + \overline{A} \cdot B$ means $A + (\overline{A} \cdot B)$, and *not* $(A + \overline{A}) \cdot B$. Write out truth tables that demonstrate that

(a) $A \cdot (\overline{A} + B) = A \cdot B$, and

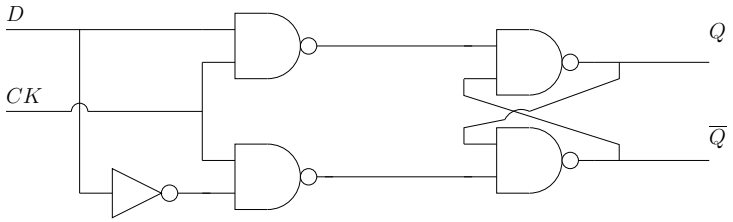
(b) $A + A \cdot B = A$

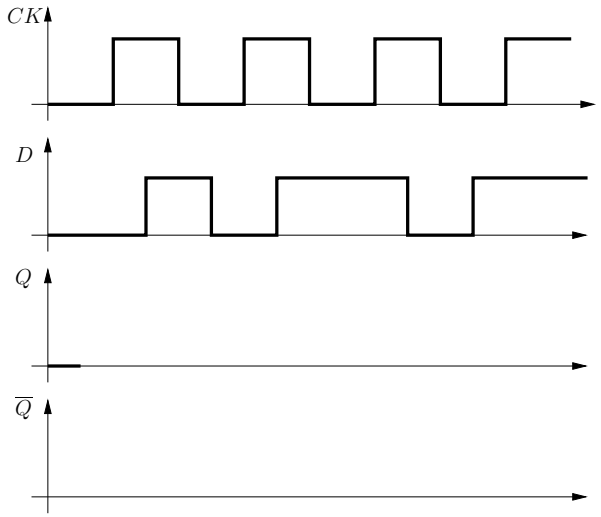
92. Sketch Q for the illustrated clocked RS flip-flop. The flip-flop PRESET and CLEAR are asynchronous. This means that they act like a SET and RESET that override the clock. Note that PRESET and CLEAR inputs are active-low.



93. (a) Write the truth table for the illustrated circuit.

    (b) Complete the timing diagram.

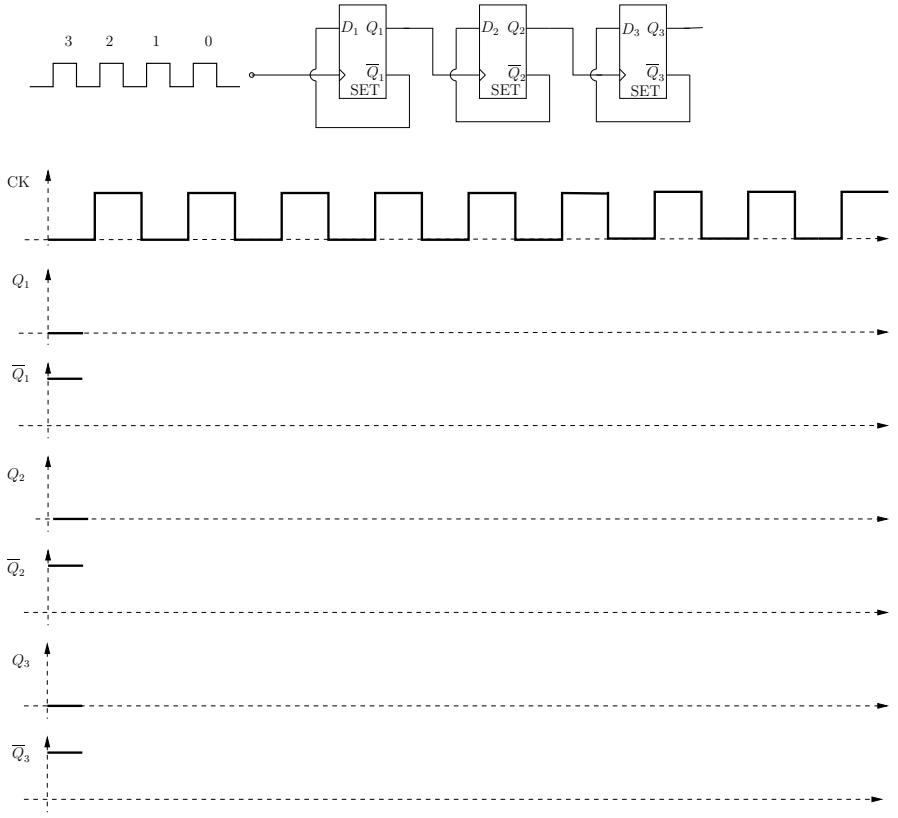




94. The illustrated circuit is made of positive edge-triggered type D flip-flops.

(a) Complete the timing diagram for the circuit.

(b) If you consider $\overline{Q}_3\overline{Q}_2\overline{Q}_1$ as a binary number, what is the counting sequence for the circuit.

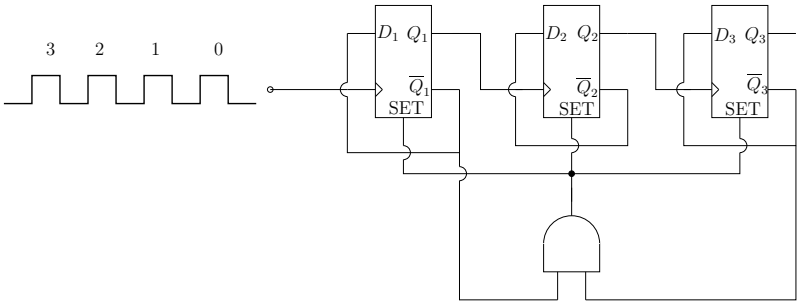


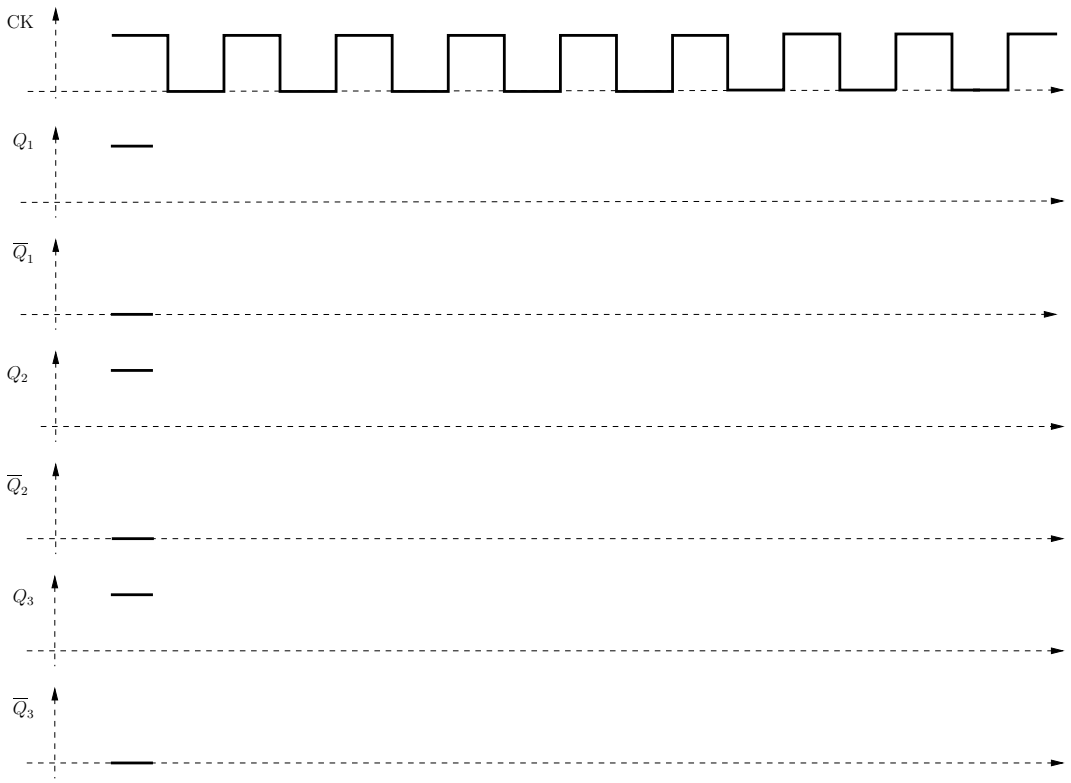
95. In lab you built a one-shot from a 555 timer chip: you connected a resistor R between 5 V and pins 6 & 7, and you connected a capacitor C between pins 6 & 7 and ground. Show that the duration of the pulse from this one-shot is $1.1RC$.

96. The illustrated circuit is made of positive edge-triggered type D flip-flops and an AND gate.

(a) Complete the timing diagram for the circuit. (You may need to consult the *CMOS Cookbook*).

(b) If you consider $\overline{Q}_3\overline{Q}_2\overline{Q}_1$ as a binary number, what is the counting sequence for the circuits.

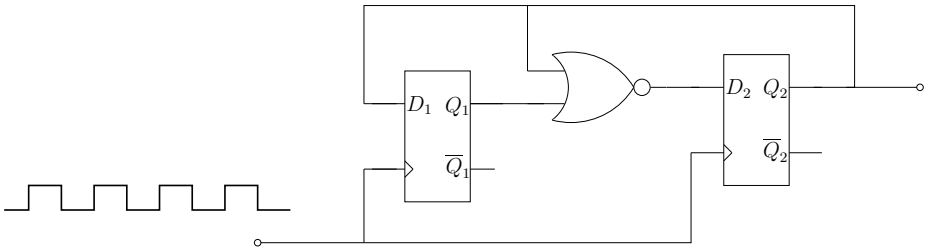


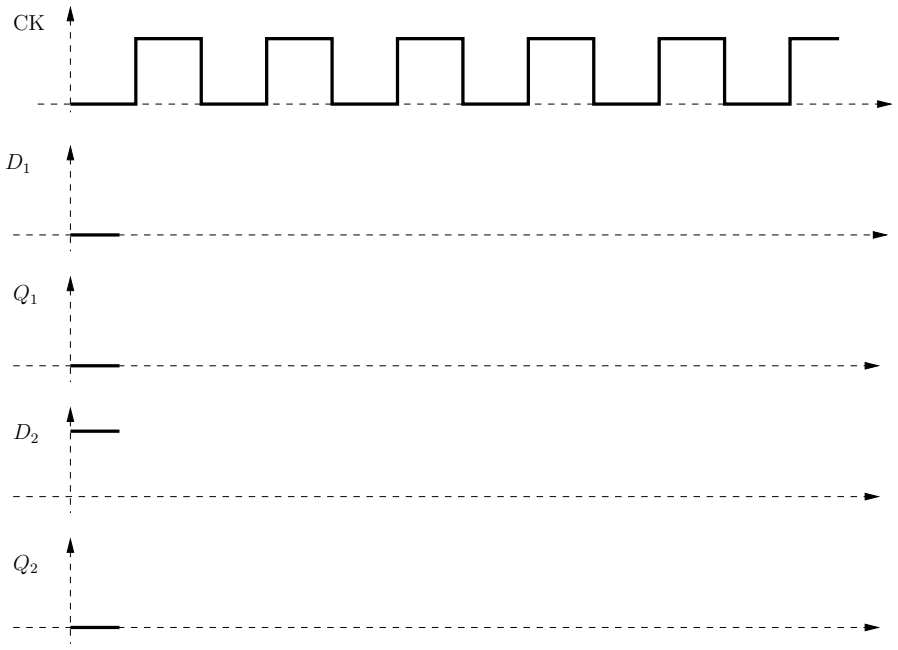


97. The illustrated circuit is made of 2 positive edge-triggered type D flip-flops and a NOR gate. Notice that the clock is applied simultaneously to both flip-flops, which makes this is an example of a *synchronous* counter in which all outputs change simultaneously. (In lab you built a *ripple*, or *asynchronous* counter, in which the output of one flip-flop serves as the clock for the next flip-flop.)

(a) Complete the timing diagram for this counter.

(b) In lab you built what are known as divide-by-2 counter and a divide-by-4 counters. What's a good name for the counter of this problem?





98. Consider an eight-bit single-slope A/D converter with $V_{\text{ref}} = 5\,\text{V}$ and $T_{\text{clock}} = 1\,\mu\text{s}$. Imagine that the converter is used to digitize an input signal of $v_{\text{in}} = 5\,\text{V}$.

    (a) If $R_{\text{integrator}} = 10\,\text{k}\Omega$, and $C_{\text{integrator}} = 0.01\,\mu\text{F}$, what is the digital output?

    (b) If $R_{\text{integrator}} = 100\,\text{k}\Omega$, and $C_{\text{integrator}} = 0.01\,\mu\text{F}$, what is the digital output?

99. Consider an eight-bit version of the dual-slope A/D converter you built in lab with $V_{\text{ref}} = 5\,\text{V}$, $T_{\text{clock}} = 1\,\mu\text{s}$, $R_{\text{integrator}} = 10\,\text{k}\Omega$, and $C_{\text{integrator}} = 0.01\,\mu\text{F}$. Imagine that the converter is used to digitize an input signal of $v_{\text{in}} = 1.25\,\text{V}$. What is the digital output?

100. If the most significant bit (MSB) of an eight-bit A/D converter corresponds to an input voltage of 5 V,

    (a) What range of analog input voltage will produce an output of 10100101?

    (b) What will the digital output be for an analog input of 8.75 V?

101. If the most significant bit (MSB) of an eight-bit D/A converter corresponds to an output voltage of 5 V,

    (a) What is the analog output for a digital input of 01100101?

    (b) What is analog output for a digital input of 10010000?

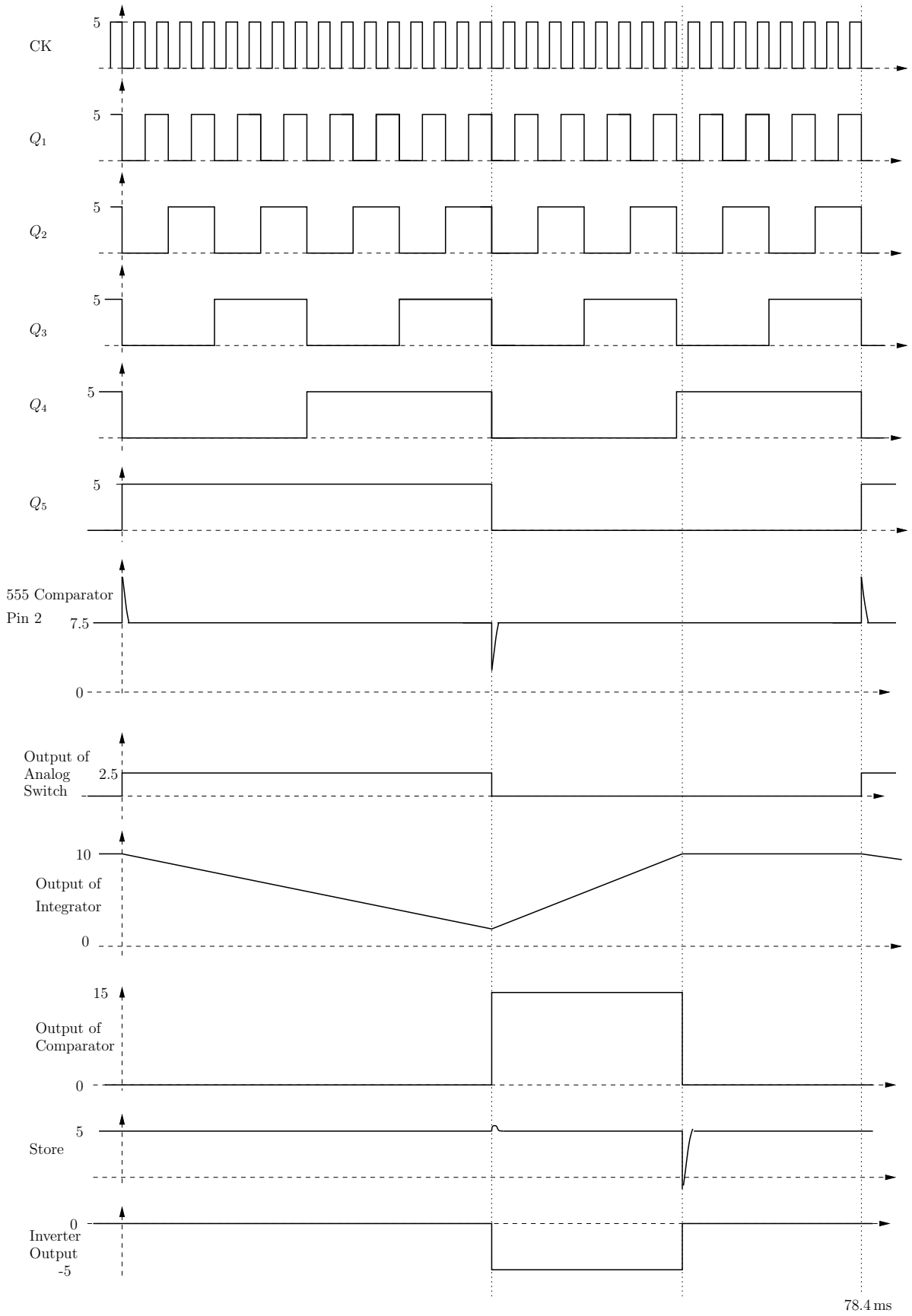
102. In lab you built a dual-slope analog-to-digital converter, and you completed a timing diagram for important signals. The following page gives a timing diagram that I made from my version of the A/D converter when I had an input voltage of 2.5 V.

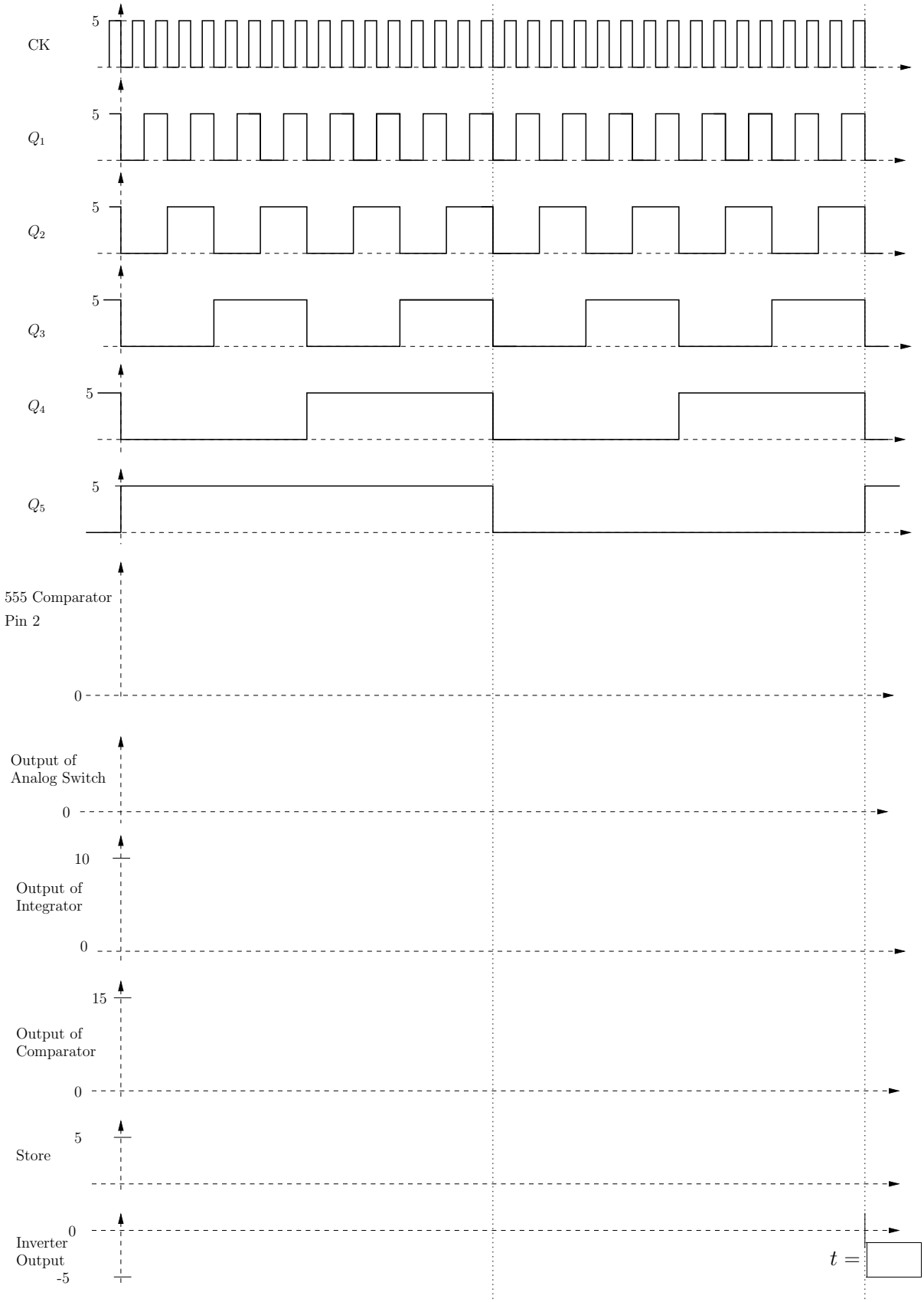
(a) What is the binary output of my A/D converter for the input voltage of 2.5 V? (This should be clear from the timing diagram.)

(b) Redraw the timing diagram for the case in which the input voltage is 1.25 V (rather than 2.5 V. What is the binary output? (A blank timing diagram is on the page following my timing diagram; print copies as needed for this and the following questions.)

(c) Now imagine returning to an input voltage of 2.5 V, but this time add an additional 0.1 μF capacitor in parallel with the capacitor in the clock. Redraw the timing diagram. What is the binary output?

(d) Imagine returning to the original capacitance in the clock, but this time add an additional 0.1 μF capacitor in parallel with the capacitor in the integrator. Redraw the timing diagram for an input of 2.5 V. What is the binary output?


CK
5
Q_1
5
Q_2
5
Q_3
5
Q_4
5
Q_5
5
555 Comparator
Pin 2
7.5
0
Output of
Analog
Switch
2.5
10
Output of
Integrator
0
15
Output of
Comparator
0
Store
5
0
Inverter
Output
-5
78.4 ms


CK
5
Q_1
5
Q_2
5
Q_3
5
Q_4
5
Q_5
5
555 Comparator
Pin 2
0
Output of
Analog Switch
0
10
Output of
Integrator
0
15
Output of
Comparator
0
5
Store
0
Inverter
Output
-5
$t =$

103. Design a digital to analog converter that will convert a three-bit binary number into an analog voltage with 000_2 corresponding to 0 V and 111_2 corresponding to 1.225 V.

104. Use a computer graphing tool to make graphs of the following sums:

(a)

$$s_a(t) = \sum_{n=1}^{1} \frac{4\left(-1^{(n+1)} + 1\right)}{(n\pi)^2} \cos(2n\pi t).$$

(b)

$$s_b(t) = \sum_{n=1}^{3} \frac{4\left(-1^{(n+1)} + 1\right)}{(n\pi)^2} \cos(2n\pi t).$$

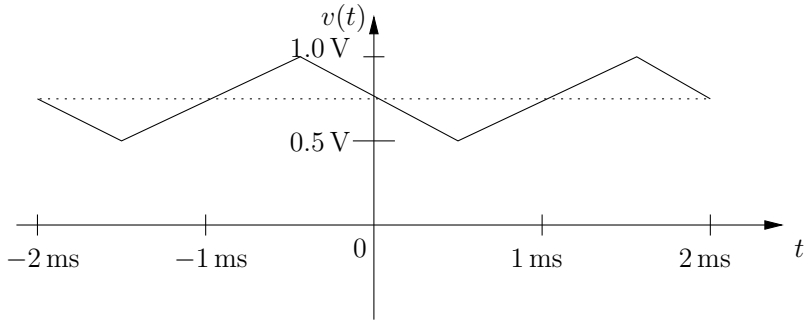
(c)

$$s_c(t) = \sum_{n=1}^{5} \frac{4\left(-1^{(n+1)} + 1\right)}{(n\pi)^2} \cos(2n\pi t).$$

(d)

$$s_d(t) = \sum_{n=1}^{101} \frac{4\left(-1^{(n+1)} + 1\right)}{(n\pi)^2} \cos(2n\pi t).$$

105. Consider the following graph of a periodic voltage signal:



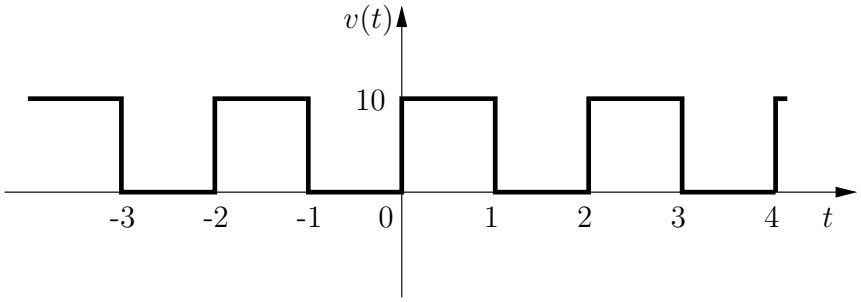
All (well-behaved) periodic signals can be represented by a Fourier series:

$$v(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos n\omega t + \sum_{m=1}^{\infty} b_m \sin m\omega t.$$

From the graph, estimate the following quantities: ω_1, a_0, a_1, b_1, and a_2. What is the sign of b_2?

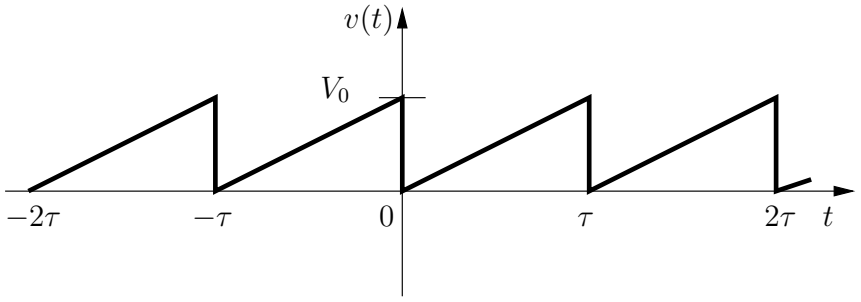
106. Fourier analyze the illustrated periodic square wave, i.e., determine values for the coefficients a_0, a_n, and b_n, and for ω, in the Fourier representation of the signal,

$$v(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos n\omega t + \sum_{m=1}^{\infty} b_m \sin m\omega t.$$



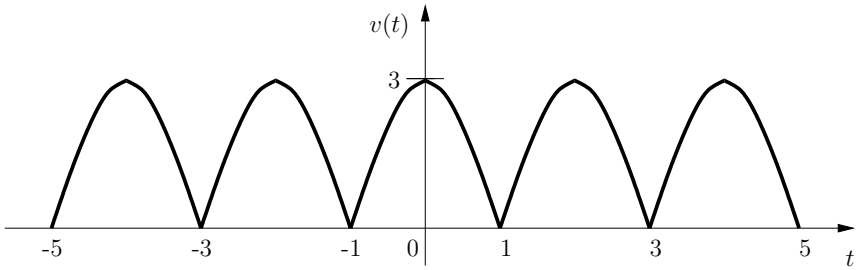
107. Fourier analyze the illustrated periodic sawtooth wave, i.e., determine expressions for the coefficients a_0, a_n, and b_n, and for ω, in the Fourier representation of the signal,

$$v(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos n\omega t + \sum_{m=1}^{\infty} b_m \sin m\omega t.$$



108. Fourier analyze the illustrated periodic signal, which is a sequence of positive half-sine waves, i.e., determine values for the coefficients a_0, a_n, and b_n, and for ω, in the Fourier representation of the signal,

$$v(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos n\omega t + \sum_{m=1}^{\infty} b_m \sin m\omega t.$$



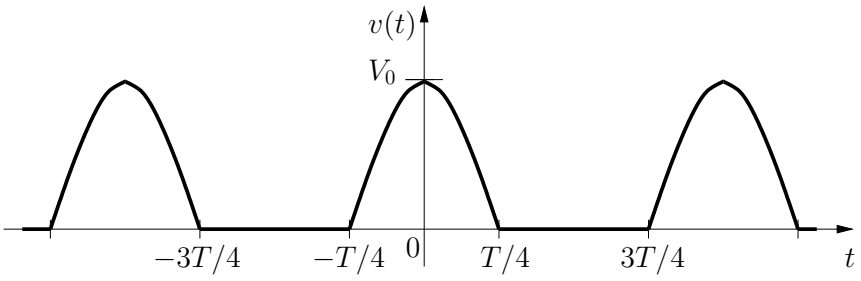
109. Fourier analyze the illustrated periodic rectified sine wave, i.e., determine expressions for the coefficients a_0, a_n, and b_n, and for ω, in the Fourier representation of the signal,

$$v(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos n\omega t + \sum_{m=1}^{\infty} b_m \sin m\omega t.$$

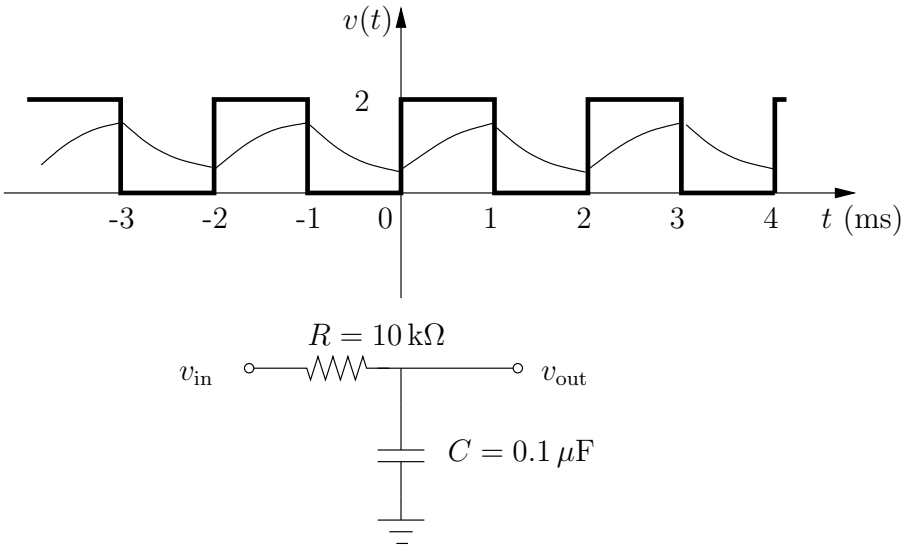
You should find that $b_m = 0$ for all values of m, and

$$a_n = \frac{2V_0}{\pi(1-n^2)} \cos\left(\frac{n\pi}{2}\right)$$

(or some equivalent expression). From this you should show that $a_0 = 2V_0/\pi$, $a_1 = V_0/2$, $a_2 = 2V_0/(3\pi)$, $a_4 = -2V_0/(15\pi)$, and for all odd values of $n > 1$, $a_n = 0$.



110. In lab you observed the output of a low-pass RC low-pass filter when the input was a square wave; the output of a 500 Hz square wave for the given filter looked something like that illustrated in the figure below. (Note that the time axis units are milliseconds.)



In this problem you will construct the output v_{out} in three steps. You will

- Fourier analyze the square wave in order to write it as a sum of sinusoidal terms (you may use previous results for similar square waves)

$$v_{\text{in}}(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos n\omega t + \sum_{m=1}^{\infty} b_m \sin m\omega t.$$

- modify each term in the Fourier decomposition according to the known action of a low-pass filter on a sinusoidal input ($a_n \to a'_n$, $b_n \to b'_n$, add appropriate phase shifts); and
- recombine the modified sinusoidal terms in a new sum.

$$v_{\text{out}}(t) = \frac{a'_0}{2} + \sum_{n=1}^{\infty} a'_n \cos(n\omega t + \phi_n) + \sum_{m=1}^{\infty} b'_m \sin(m\omega t + \phi_m).$$

Complete the table below, and make graphs of your Fourier series approximation of v_{out} using 1, 2, 3, and "many" non-zero terms in your series.

$n\ (m)$	a_n	b_m	a'_n	b'_m	ϕ
0		XXX		XXX	XXX
1					
2					
3					
formula					

March 30, 2015