CSCI 315 Operating Systems Design
Activity 18

These exercises are slightly modified versions of those in our textbook *Operating Systems Concepts,* by Silberschatz, Galvin, and Gagne, 9th. ed.

Work with one or two partners in this activity.

1) Consider a memory system implemented with paging. Assume that the size of a page is 1 KB (that is, 1,024 bytes). Determine the page number and the offset for the following address references:
    a) 3,085
    b) 42,095
    c) 2,000,001

2) Consider a memory system with 21-bit *logical addresses* that uses paging with page size of 2 KB.
    a) If physical addresses have 16 bits, determine the maximum amount of physical memory that can be installed in the system.
    b) Determine the number of entries in the page table when a single-level structure is used.
    c) Imagine that you want to implement a two-level hierarchical structure of page tables. Assume that you want to have a roughly equal number of entries in the page tables at both levels. Determine the number of bits used to index the page tables in level 1, the number of bits used to index the pages tables in level 2, and the number of bits for the offset in the logical address.

3) Consider a logical address space of 256 pages with a 4 KB page size, mapped onto a physical memory of 64 frames.
    a) Determine the number of bits in the logical address.
    b) Determine the number of bits in the physical address.

4) Use the base table below to determine the physical addresses for the given logical addresses. The addresses given to you are in format <segment#, offset>.

Segment	Base	Length
0	219	600
1	2300	14
2	90	100
3	1327	580
4	1952	96

    a) <0,430>
    b) <1,110>
    c) <2,500>
    d) <3,400>
    e) <4,112>