ECEG 350 **Electronics I** **Fall 2024**

Policies and Review Topics for Exam #2

The following policies will be in effect for the exam. They will be included in a list of instructions and policies on the first page of the exam:

1. You will be allowed to use a non-wireless enabled calculator, such as a TI-99.
2. You will be allowed to use two 8.5 × 11-inch two-sided handwritten help sheets. No photocopied material or copied and pasted text or images are allowed. If there is a table or image from the textbook or some other source that you feel would be helpful during the exam, please notify me.
3. All help sheets will be collected at the end of the exam but will be returned to you later.
4. If you begin the exam after the start time, you must complete it in the remaining allotted time. However, you may not take the exam if you arrive after the first student has completed it and left the room. The latter case is equivalent to missing the exam.
5. **You may not leave the exam room without prior permission except in an emergency or for an urgent medical condition. Please use the restroom before the exam.**

For students in the 1:00 pm lab section, the exam will take place 1:00–2:50 pm on Tuesday, October 29 in Dana 134. For students in the 3:00 pm lab section, the exam will take place 3:00–4:50 pm on Tuesday, October 29 in Breakiron 165.

The following is a list of topics that could appear in one form or another on the exam. Not all of these topics will be covered, and it is possible that an exam problem could cover a detail not specifically listed here. However, this list has been made as comprehensive as possible. You should be familiar with the topics on the previous review sheet in addition to those listed below.

Although significant effort has been made to ensure that there are no errors in this review sheet, some might nevertheless appear. The textbook and the supplemental readings are the final authority in all factual matters, unless errors have been specifically identified there. You are ultimately responsible for obtaining accurate information when preparing for the exam.

Op-amp slew rate (S.R.) limit (max. slope of output voltage vs. time)

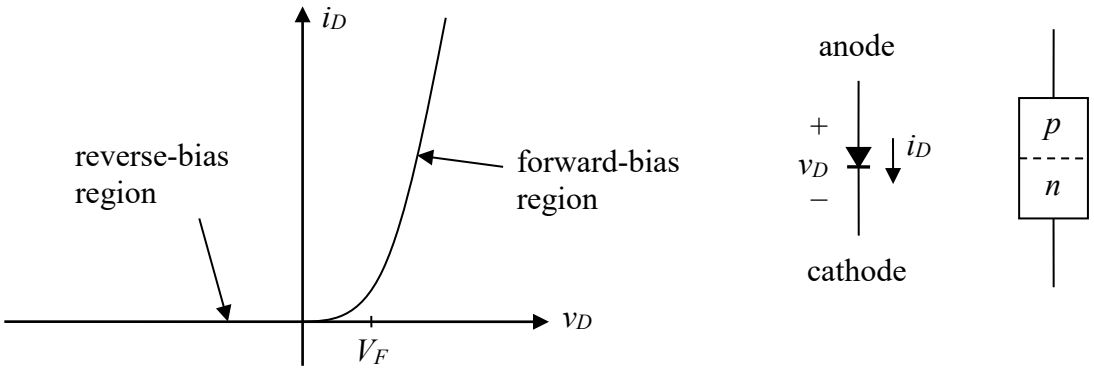
- slope of output voltage = dv_o/dt
- to avoid slew rating limiting, must ensure at all times that $\left|\frac{dv_o}{dt}\right|_{\max} \le \text{S.R.}$
- slope of some parts of waveform might be less than slew rate, but output might need to "catch up" from earlier time interval when slew rate was exceeded
- slew rate limiting, when it occurs, can cause distortion of output voltage waveform
- slew rate limiting can be a significant issue with high-frequency signals
- virtual short disappears when slew rate is exceeded; circuit cannot react to changes
- how to find voltage across op-amp inputs when slew rate limiting occurs
- the expression below is valid **ONLY** for sinusoidal signals:

$$f_{\max} = \frac{\text{S.R.}}{2\pi v_{O\max}}$$

Semiconductors based on silicon (Si)

- holes and electrons
- acceptor and donor impurities (group III and V elements on the periodic chart)
- *n*-type vs. *p*-type material
- free charges vs. immobile charges (ions locked in crystal structure)
- depletion region and the built-in field
- diffusion current vs. drift current

pn-junction diode operation



- in the symbol, the bar and the forward sides of the arrow form a "K" for "kathode"
- basic construction; doping of pure silicon with Group III and V elements
- diode symbol and correct orientation
- reverse bias enhances built-in electric field across depletion region and therefore prevents current flow via diffusion; electric field force exceeds diffusion "force"
- forward bias suppresses built-in electric field across depletion region and therefore allows current to flow, primarily through diffusion of holes and electrons
- *i*-*v* characteristic and orientation of i_D and v_D relative to diode symbol
- graphical and iterative analyses of diode circuits (load lines and/or transcendental equations)
- diode equation: $i_D = I_S\left(e^{v_D/\eta V_T} - 1\right)$,

  where I_S = scale or saturation current, η = emission coefficient, and V_T = thermal voltage

  $V_T = \dfrac{T}{11{,}600}$, where T = temperature in kelvins

  I_S is very small (10^{-15} to 10^{-8} A) but proportional to junction area

  η = 1 to 2 for most Si diodes (different values for other types); empirically determined values of η and V_F are very different for light-emitting diodes (LEDs) and depend on color

Piecewise linear (PWL) diode models (applicable to *pn*-junction and zener types)

- turn-on (V_F) voltage
- diode behavior along different segments of PWL *i*-*v* characteristic
- [not on exam, but good to know:] forward (r_d) and zener (r_Z) resistances
- [not on exam, but good to know:] dependence of forward resistance on avg. (DC) diode current:

  $r_d = \dfrac{\eta V_T}{i_D} \approx \dfrac{\eta V_T}{I_D}$,

  where i_D = total diode current (AC + DC); I_D = quiescent diode current (DC only)

Constant-voltage diode model (special case of the piecewise linear diode model)

- simplest PWL model other than ideal model & adequate for most analyses
- ideal diode model is the constant-voltage model with $V_F = 0$
- ON state: diode acts like voltage source; $v_D = V_F$ (behavior) and $i_D > 0$ (check)
- OFF state: diode acts like an open; $i_D = 0$ (behavior) and $v_D < V_F$ (check)
- for analysis, assume state of each diode, which dictates its behavior, and perform normal linear circuit analysis. Then verify (check) each assumed diode state. If validity of assumption is confirmed, then analysis is done; if not, then one or more diodes are in the opposite state.

Rectifier circuits

- half-wave rectifiers
- full-wave rectifiers (bridge and with center-tapped transformer)
- pulsating DC and its average value
- effect of diode voltage drop(s) on output voltage of rectifier
- diode on/off states change over period of AC waveform
- relationships between frequency (f), radian frequency (ω), and period (T) of AC waveforms
- transformer secondary voltage selection; understand differences b/w pk, rms, and peak-to-peak (pp) voltages and how to convert between them
- full secondary voltage vs. voltages between ends of winding and center-tap
- peak reverse (inverse) voltage and PRV (or PIV) ratings of diodes
- effects of diode failures (when failed diodes act as open circuits)

Power supply ripple filters

- filter capacitor selection vs. equiv. load resistance and/or load current (V_P = peak value of output voltage, V_r = ripple voltage), and derivation of formulas:

  $$C_{\min} = \frac{1}{f R_{L\min}\left(V_r / V_P\right)} \approx \frac{i_{L\max}}{f V_r} \text{ (half-wave rectifier)}$$

  $$C_{\min} = \frac{1}{2 f R_{L\min}\left(V_r / V_P\right)} \approx \frac{i_{L\max}}{2 f V_r} \text{ (full-wave rectifier, center-tapped or bridge)}$$

  based on $i_c = C\frac{dv_c}{dt} \approx -C\frac{V_r}{0.5T}$ (full-wave rectifier) or $-C\frac{V_r}{T}$ (half-wave rectifier), where i_c, v_c = capacitor current and voltage; T, f = period and frequency of AC waveform
- ripple voltage, percentage ripple, and fractional ripple
- interpretation of $i_{L\max}$ in $C_{\min}$ formula; it represents all of the current that the capacitor must supply during its discharge interval; the "L" in the subscript refers to the load on the capacitor, not just the load on the power supply (power supply's load might be a subset of capacitor's load)
- selection of bleeder resistor for filter capacitor
- peak diode current:

  $$i_{D\max} = I_L\left(1 + 2\pi\sqrt{2V_{\text{sec,pk}} / V_r}\right) \text{ (half-wave rectifier)}$$

  $$i_{D\max} = I_L\left(1 + 2\pi\sqrt{V_{\text{sec,pk}} / 2V_r}\right) \text{ (full-wave rectifier)}$$

  where $V_{\text{sec,pk}}$ = peak value of transformer's secondary winding voltage for half-wave and full-wave bridge rectifiers or peak value of secondary half-voltage for full-wave rectifier with center tap; V_r = ripple voltage

- average diode current (averaged only over the conduction interval):
  $i_{Dav} = I_L\left(1+\pi\sqrt{2V_{\text{sec,pk}}/V_r}\right)$ (half-wave rectifier)
  $i_{Dav} = I_L\left(1+\pi\sqrt{V_{\text{sec,pk}}/2V_r}\right)$ (full-wave rectifier)
- individual diode conduction time (for both half and full-wave rectifiers)
  $\Delta t = \frac{1}{\omega}\sqrt{\frac{2V_r}{V_{\text{sec,pk}}}} = \frac{1}{2\pi f}\sqrt{\frac{2V_r}{V_{\text{sec,pk}}}} = \frac{T}{2\pi}\sqrt{\frac{2V_r}{V_{\text{sec,pk}}}}$,
  where $V_{\text{sec,pk}}$ and V_r have the same definitions as above

Voltage regulation

- advantages over simple rectifier/filter design:
  - reduces output ripple voltage without using excessively large filter capacitor for a given load current
  - mitigates effects of variable power line (AC) voltage
  - mitigates effects of uncertainty (tolerance) of diode voltage drops, transformer secondary voltage, and internal resistances of transformer and diodes
- selection of bleeder resistor for filter capacitor in regulator circuits

Three-terminal voltage regulators (like the LM117 and LM317)

- selection of filter capacitors in regulator circuits
  - $V_{\max} = v_{\text{sec,pk}} - 2V_F$, where V_F = rectifier diode turn-on voltage
  - $V_{\min} = \left(\text{Buffer Factor}\right)\left(v_{O\max} + V_{DO}\right)$,
    where "Buffer Factor" = 1.4 to 1.8 (sets $V_{\min}$ value 40% to 80% higher than $v_{O\max} + V_{DO}$), $v_{O\max}$ = nominal output voltage, and V_{DO} = drop-out voltage of regulator
  - target filter capacitor ripple for max. load current: $V_{rC} = V_{\max} - V_{\min}$
  - trade-off between capacitor value and transformer secondary voltage
  - time-average power dissipation of regulator and possible need for heat sink
- input current (often labeled i_I) of three-terminal regulator is approximately equal to load current (often labeled i_L), especially at maximum rated load current
- regulators usually require a minimum output current (typically around 5–10 mA) to maintain specified output voltage
- relatively small capacitors (typically a few tenths of a μF to 1 μF) are sometimes mounted close to input and output terminals of regulator to maintain stability and suppress transient responses in practical circuits
- output voltage regulation can suffer if regulator device gets hot enough to activate internal protection circuitry
- output voltage regulation can also suffer if significant stray resistance is present between output terminal of regulator and load (stray resistance increases load regulation by an amount equal to the stray resistance)

Load regulation

- definition: load regulation = $\frac{\Delta v_O}{\Delta i_L}$,
  where Δv_O is change in output voltage for given change in load current Δi_L for constant regulator input voltage v_I ("output" and "load" refer to the same thing)
- conversion of load regulation unit used in datasheets (% unit) to the mV/mA unit and vice versa

- load regulation is essentially the Thévenin equivalent (internal) resistance of the output port of the regulator
- load regulation is effectively increased by the resistance of the conductors (such as circuit board traces) between the regulator output terminals and the load; stray resistance of the output conductors degrades load regulation by increasing its value

Line regulation

- definition: line regulation = $\frac{\Delta v_O}{\Delta v_I}$,

  where Δv_O is change in output voltage for given change in line (input) voltage Δv_I for constant load current i_L (Δv_I is usually equal to the ripple on filter capacitor voltage)
- conversion of line regulation unit used in datasheets (% unit) to the mV/V unit
- line regulation can be thought of as the ripple suppression or attenuation of the regulator; the ripple voltage on the filter capacitor on the input side is greatly reduced by the regulator so that the ripple voltage at the load on the output side is very small; i.e., the output ripple is a scaled down version of the input ripple
- When i_L increases, the capacitor and output ripple increase, and the time-average (and peak) output voltage drops.

Relevant course material:

HW:	#5 and #6
Labs:	#3
Readings:	Assignments from Sept. 25 through Oct. 23 (except Chap. 5 readings), including the lecture notes: "Brief Explanation of Slew Rate Limiting in the LM741 Operational Amplifier" "Average and Peak Diode Currents in Rectifier Circuits" "Voltage Regulation and Power Conversion" "Three-Terminal Linear Voltage Regulators"

This exam will focus primarily on the course outcomes listed below and related topics:

1. Predict and/or mitigate the effects of the nonideal properties of operational amplifiers on circuit performance. [only slew rate limiting]
3. Analyze and/or design circuits involving diodes using the piecewise linear diode model.
4. Analyze and/or design power supply circuits using linear voltage regulators.

The course outcomes are listed on the Course Policies and Information sheet, which was distributed at the beginning of the semester and is available on the Syllabus and Policies page at the course web site. The outcomes are also listed on the Course Description page. Note, however, that some topics not directly related to the course outcomes could be covered on the exam as well.