ECEG 350 **Electronics I** **Fall 2024**

Final Exam General Information

The first page of the exam will include a detailed list of instructions and policies. You should especially note the following:

1. You will be allowed to use a non-wireless enabled calculator, such as a TI-99.
2. You will be allowed to use up to four 8.5 × 11-inch two-sided handwritten help sheets. No photocopied material or copied and pasted text or images are allowed. If there is a table or image from the textbook or some other source that you feel would be helpful during the exam, please notify me.
3. All help sheets will be collected at the end of the exam but will be returned to you upon request.
4. If you begin the exam after the start time, you must complete it in the remaining allotted time. However, you may not take the exam if you arrive after the first student has completed it and left the room. The latter case is equivalent to missing the exam.
5. **You may not leave the exam room without prior permission except in an emergency or for an urgent medical condition. Please use the restroom before the exam.**

Rough breakdown of topic coverage (two topics possibly combined into one problem):

1–2 problems	NMOS and/or PMOS channel-length modulation (r_o)
1–2 problems	NMOS and/or PMOS source follower and/or common-gate circuits
1–2 problems	PMOS regions of operation and bias design
1–2 problems	CMOS logic gate circuits
1 problem	Basic BJT circuit analysis (DC/bias only or switching circuits)

The final exam is not cumulative in the sense that you will not be presented with problems whose solutions relate specifically to the material covered before Exam #3. However, much of the material that was covered since then builds on the earlier material. (For example, you should know at a basic level how *pn*-junctions work, and you should be able to determine the region of operation of a MOSFET. A problem might include one or more diodes in the circuit.) You will be expected to have a solid grasp of foundational concepts that are relevant to the material covered in the last few weeks of the semester.

The final exam will take place **3:30–6:30 pm on Tuesday, December 17 in Breakiron 264**. The exam will be designed to be completed in just over one hour, but you may use the full three hours. **You must begin the exam at 3:30 pm.** You will not be allowed to take the exam if you arrive after the first student has completed it and left the room.

The final exam score, like the mid-semester exam scores, will be eligible for reduced weighting when the overall average score for the semester is calculated. If your final exam score is lower than your three mid-semester exam scores, then it will be weighted only 5% instead of 20%.

Solutions to the final exam will not be posted, but you may review your final exam and discuss it with me at any time after it has been graded, even next year. Your final exam score will be posted at the course Moodle site.

Review Topics for ECEG 350 Final Exam

The following is a list of topics that could appear in one form or another on the exam. Not all of these topics will be covered, and it is possible that an exam problem could cover a detail not specifically listed here. However, this list has been made as comprehensive as possible. You should be familiar with the topics on the previous review sheets in addition to those listed below.

Although significant effort has been made to ensure that there are no errors in this review sheet, some might nevertheless appear. The textbook is the final authority in all factual matters, unless errors have been specifically identified there. You are ultimately responsible for obtaining accurate information when preparing for your exam.

Finite output (drain-to-source) resistance r_o of MOSFETs (channel-length modulation)

- represents slope of i_D-v_{DS} characteristic in the saturation region due to channel-length modulation (sometimes referred to as the Early effect, although that term technically applies only to BJTs)
- channel-length modulation parameter: $\lambda = \dfrac{1}{V_A + V_{OV}} \approx \dfrac{1}{V_A}$,
  where V_A = Early voltage
- $r_o \approx \dfrac{V_A}{I_D} \approx \dfrac{1}{\lambda I_D}$, where I_D is the quiescent drain current
- r_o is typically 20–100 kΩ for MOSFETs but can be much lower for some types, especially integrated MOSFETs; it can be a major factor limiting amplifier gain
- r_o is <u>not</u> equal to r_{DS} of MOSFET in low-v_{DS} triode region! r_o is only relevant in the saturation region
- *i*-*v* characteristic in saturation region that includes λ:
  $i_D = \dfrac{1}{2} k_n v_{OV}^2 \left[1 + \lambda\left(v_{DS} - v_{OV}\right)\right] \approx \dfrac{1}{2} k_n v_{OV}^2 \left(1 + \lambda v_{DS}\right)$, where $v_{OV} = v_{GS} - V_t$

Source follower circuits

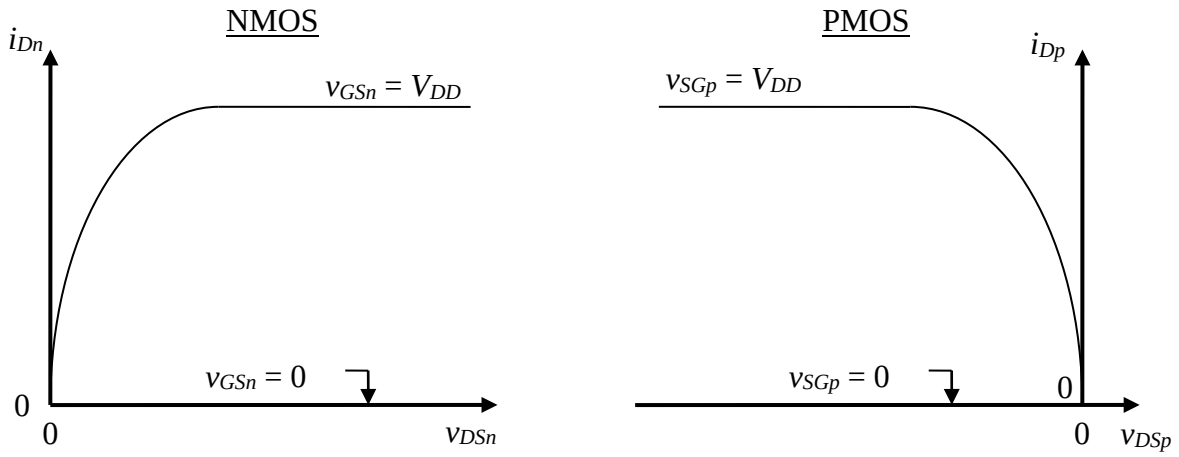
- less commonly called a *common-drain* amplifier
- voltage gain is positive and less than unity (one), but current gain (and therefore power gain) can be very high
- voltage transfer characteristic (v_o vs. v_{in}) has positive slope in saturation region because gain is positive
- output is taken from source terminal of MOSFET; output resistance ≈ $1/g_m$ (typically, 10s to 100s of ohms)
- not necessary to include a resistor between drain terminal and V_{DD} (for NMOS) or between drain terminal and ground (for PMOS)
- can design source followers using NMOS or PMOS devices; small-signal model is the same for either device

Common-gate amplifier

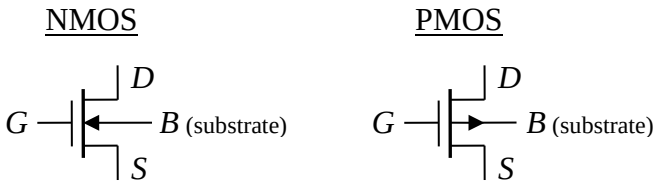
- noninverting
- gain comparable to common-source amp; $A_v = g_m(r_o \| R_D \| R_L)$ in the typical circuit design
- gate terminal can be grounded directly (requires a bipolar power supply) or for signals only through a capacitor (capacitor blocks DC)
- input resistance ≈ $1/g_m$ (typically, 10s to 100s of ohms)

n-channel vs. *p*-channel MOSFETs (NMOS and PMOS)

- comparison of electron mobility μ_n vs. hole mobility μ_p (hole mobility is approximately 0.25 to 0.5 times electron mobility for doped Si); thus, NMOS is faster than PMOS, and NMOS amps generally have more gain than PMOS amps for a given quiescent drain current
- v_{GS}, v_{DS}, and V_t are all negative for enhancement-mode PMOS, so v_{SG}, v_{SD}, and $|V_t|$ are often used in formulas instead
- i_D is positive for both types (Sedra and Smith's convention), so i_{Dn} flows *into* the drain of an NMOS device, and i_{Dp} flows *out of* the drain of a PMOS device
- *i-v* characteristics of NMOS and PMOS; v_{DSp} is negative; curves for v_{GSn} or v_{SGp} with magnitudes less than V_{DD} lie between the horizontal axis and the ones for V_{DD}:



- circuit symbols (enhancement-mode shown; pay attention to directions of arrows; PMOS symbol is often drawn "upside-down" with source terminal above drain terminal in circuit diagrams):



substrate (or body) internally connected to source (discrete devices):

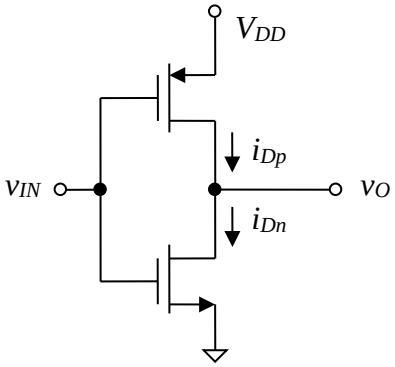
Symbols frequently used in digital logic gate literature:

- small-signal model is the same for NMOS and PMOS devices

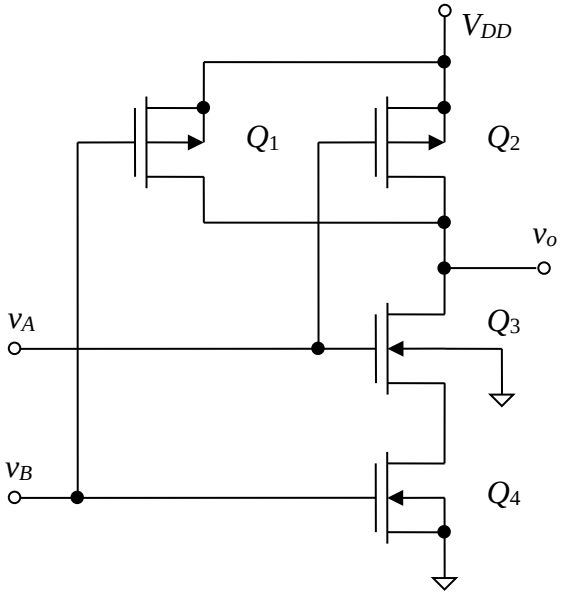
CMOS logic gates

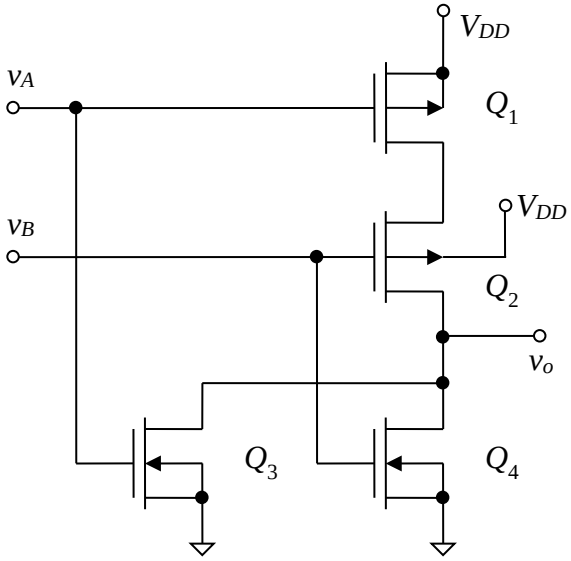
- no resistors used
- $i_{Dp} \approx 0$ and $i_{Dn} \approx 0$; i.e., negligible drain current once equilibrium is established after logical state change (assumes no significant current supplied to load connected to output terminal); true for *all* types of CMOS gates
- MOSFETs are in either cut-off ("off") or triode region ("on") in all logical states after equilibrium is reached
- MOSFETs in triode region have $v_{DS} = 0$ because $i_D = 0$ in equilibrium
- MOSFETs in cut-off region can have $v_{DS} = 0$, $v_{DS} = V_{DD}$, or any other voltage
- during logical transitions, significant drain current flows and reaches a peak when MOSFETs are in the saturation region; the primary source of time-average dissipated power in CMOS gates is the brief current that charges/discharges gate capacitance of following logic gates through the drain-to-source resistance r_{DS} (hundreds to a few thousand ohms) that characterizes the triode region; comparatively less dissipation in r_o in the saturation region
- CMOS inverter circuit (shown at right); as v_{IN} increases from 0 V to V_{DD}, the regions of operation progress through the following states:

PMOS: triode	NMOS: cut-off
PMOS: triode	NMOS: saturation
PMOS: saturation	NMOS: saturation
PMOS: saturation	NMOS: triode
PMOS: cut-off	NMOS: triode



- NAND and NOR gate circuits:



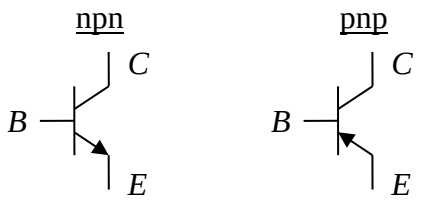


Fundamentals of BJT operation (focus is on *npn* type)

- *npn*: thin *p*-type base sandwiched between *n*-type emitter and collector
- *pnp*: opposite of *npn*
- base-emitter (B-E) and collector-base (C-B) junctions are regular *pn* junctions and have many similarities to *pn* junction diodes (i.e., they can be forward or reverse-biased; they have turn-on voltages)
- turn-on voltage (V_F) is approx. 0.7 V for Si
- effect of changing base current i_B
- effect of changing collector-emitter voltage v_{CE} (normally C-B junction is reverse biased or at least not heavily forward biased; necessary for collector current to flow)
- directions and polarities of important currents and voltages (i_B, i_C, i_E, v_{BE}, v_{CE})
- thin base region allows electrons (*npn*) or holes (*pnp*) to flow from emitter to collector
- emitter more heavily doped than base – allows base to fill with minority charge carriers (electrons for *npn*; holes for *pnp*) when base current flows; minority carriers are electrons in a *p*-type base or holes in an *n*-type base
- base-emitter junction is forward biased if v_{BE} is at turn-on voltage (V_F)
- *i*-*v* characteristic of B-E junction is the same as that of a *pn*-junction diode:
  $i_B = I_{SB}\left(e^{v_{BE}/\eta V_T} - 1\right)$,
  where I_{SB} = saturation (scale) current of B-E junction, η = emission coefficient (typically assumed to equal one), and V_T = thermal voltage, which is given by
  $V_T = \dfrac{T}{11{,}600}$, where T = temperature in kelvins ($V_T \approx 25$ mV at room temp.)
- collector-base junction is usually reverse biased (produces depletion region) or lightly forward biased; in either case, the built-in E field across the C-B junction is sufficiently strong to draw most of the minority carriers in the base into the collector
- collector current related to base current by $i_C = \beta i_B$ in the active region, where β = forward DC current gain (values are typically 20–300, but vary among BJT types, even among individual units of a given type within the same manufacturing batch)
- β varies strongly with temperature

BJT circuit symbols

pay attention to directions of arrows (arrow indicates the emitter terminal and BJT type; arrow of *npn* is "*n*ot *p*ointing i*n*"; arrow indicates direction of emitter current)



npn vs. *pnp* BJTs

- v_{BE} and v_{CE} of *npn* BJTs have positive values in normal operation
- v_{BE} and v_{CE} of *pnp* BJTs have negative values in normal operation (use v_{EB} and v_{EC}, which are positive, instead)
- i_B and i_C flow *into* base and collector terminals of *npn* BJTs and *out of* base and collector terminals of *pnp* BJTs
- i_E flows *out of* emitter terminal of *npn* BJTs and *into* emitter terminal of *pnp* BJTs
- *i*-*v* characteristics of *npn* and *pnp* BJTs have voltages of opposite sign (unless v_{EB} and v_{EC} are used for *pnp*)

General analysis techniques for BJT circuits

- during normal operation, v_{CE} (for *npn* BJTs) is always positive (negative for *pnp*; i.e., v_{EC} is positive for *pnp*)
- $v_{BE} \approx 0.7$ V (for Si *npn*) in the active and saturation regions ($v_{EB} \approx 0.7$ V for Si *pnp*)
- regions of operation for silicon *npn* BJTs ($v_{CE}|_{\text{sat}} \approx 0.2$–$0.3$ V):
  - cut-off: $v_{BE} < 0.7$ V, $i_B = i_C = 0$
  - active: $v_{BE} \approx 0.7$ V, $i_C = \beta i_B$ and $v_{CE} > v_{CE}|_{\text{sat}}$
  - saturation: $v_{BE} \approx 0.7$ V, $i_C < \beta i_B$ and $v_{CE} = v_{CE}|_{\text{sat}}$
- determination of region of operation (cutoff, active, or saturation)
  - if possible, determine whether base-emitter junction is forward biased; if not, then the BJT is in the cut-off region; if so, then active or saturation
  - assume BJT is in one region and analyze the circuit based on that assumption
  - check all voltages and currents and determine whether their values are consistent with the initial assumption. If so, analysis is complete. If not, use the results of the initial analysis to determine likely region of operation. Repeat analysis under new assumption and confirm.
- for more accurate analysis in active region (rarely necessary), use
  $i_B = I_{SB} e^{v_{BE}/\eta V_T}$ and $i_C = \beta I_{SB} e^{v_{BE}/\eta V_T}$ (omit "–1" because B-E junct. is forward biased),
  where I_{SB} = saturation (scale) current for B-E junction, η = emission coefficient (typically assumed to equal one), and V_T = thermal voltage
- by KCL, $i_E = i_B + i_C$ (for *npn* and *pnp*)

Relevant course material:

HW: #9 and #10 (#10 is ungraded)
Labs: #5
Readings: Assignments from Nov. 11 through Dec. 9

This exam will focus primarily on the following course outcomes and related topics:

5. Determine the region of operation of a MOSFET or BJT [focus on PMOS and BJTs].
6. Determine and/or set the bias point (quiescent operating point) of a MOSFET or BJT circuit. [focus on PMOS and simple BJT circuits]
7. Find transfer functions of basic MOSFET and/or BJT amplifier circuits, switching circuits, and digital logic circuits [focus on PMOS devices, CMOS digital circuits, and NMOS or PMOS common-gate amps and source followers, possibly with FET output resistance r_o].

The course outcomes are listed on the Course Policies and Information sheet, which was distributed at the beginning of the semester and is available on the Syllabus and Policies page at the course web site. The outcomes are also listed on the Course Description page. Note, however, that some topics not directly related to the course outcomes could be covered on the exam as well.