Policies and Review Sheet for Final Exam

The following policies will be in effect for the exam. They will be included in a list of instructions and policies on the first page of the exam:

1. You will be allowed to use a non-wireless enabled calculator, such as a TI-99.
2. You will be allowed to use up to **four** 8.5 × 11-inch two-sided handwritten help sheets. No photocopied material or copied and pasted text or images are allowed. If there is a table or image from the textbook or some other source that you feel would be helpful during the exam and that is not included on the formula sheet that I will provide, please notify me.
3. All help sheets will be collected at the end of the exam but will be returned to you later if you wish to have them back.
4. If you begin the exam after the start time, you must complete it in the remaining allotted time. However, you may not take the exam if you arrive after the first student has completed it and left the room. The latter case is equivalent to missing the exam.
5. **You may not leave the exam room before completing your exam without prior permission except in an emergency or for an urgent medical condition. Please use the restroom before the exam.** If you have a medical condition that might require you to leave the room, you must notify me before the exam begins. Only one student at a time may be absent from the room and must leave any electronic devices in the room.

The final exam will take place **7:30–10:30 pm on Thursday, May 2 in Academic East 225**.

Your graded final exam will not be returned to you, nor will the solutions be posted. However, you may make an appointment with me at any time to review your final exam and discuss your performance on it. I will keep your final exam at least until you graduate from Bucknell.

Review Topics for Final Exam

The following is a list of topics that could appear in one form or another on the exam. Not all of these topics will be covered, and it is possible that an exam problem could cover a detail not specifically listed here. However, this list has been made as comprehensive as possible. **You should be familiar with the topics on the review sheets for the previous exams as well for background material.**

Although significant effort has been made to ensure that there are no errors in this review sheet, some might nevertheless appear. The textbook and the supplemental readings are the final authority in all factual matters, unless errors have been specifically identified there. You are ultimately responsible for obtaining accurate information when preparing for your exam

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Internal capacitances in MOSFETs – **NOT COVERED ON SPRING 2024 FINAL EXAM**

- gate-source capacitance C_{gs} typically tens of pF for discrete FETs, much smaller (fF) for FETs on IC chips
- gate-drain capacitance C_{gd} and drain-source capacitance C_{ds} typically a few pF for discrete FETs, a few fF for FETs on IC chips
- short-circuit current gain (drain shorted to source; for theoretical purposes, not practical):
$$\frac{I_o}{I_i} = \frac{g_m}{j\omega\left(C_{gs} + C_{gd}\right)}$$
- unity-gain frequency or transition frequency:
$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)}$$

Switching regulators

- many types have been designed; four major types considered in this course:
    - DC buck converters (output voltage < input voltage)
    - DC boost converters (output voltage > input voltage)
    - DC buck-boost (or inverting) converters (output voltage = $-k \times$ input voltage, where $k < 1$ for buck converters or $k > 1$ for boost converters)
    - DC-to-AC converters (sometimes called inverters)
- advantages
    - linear regulators can only reduce voltage, but switching regulators are the only widely available method to increase voltage, to produce AC from DC, or to produce negative DC voltages from positive DC voltages
    - better efficiency than linear regulators
    - less weight, smaller size than linear regulators (often no transformer needed; often no large heatsink needed)
- disadvantages
    - potential for radiating electromagnetic noise or producing noise on power bus/power line; therefore, extensive filtering needed
    - possible presence of transients (e.g., spikes, discontinuities) in output voltage
    - high-quality (and therefore high-cost) inductor needed to maximize efficiency
    - greater circuit complexity, esp. to address noise issues & to provide feedback for voltage control

- analysis tools
  - assumptions of small inductor current ripple and capacitor voltage ripple
  - inductor volt-second balance

    $$v_L(t) = L\frac{di(t)}{dt} \quad \rightarrow \quad i(t+T_s) - i(t) = \frac{1}{L}\int_t^{t+T_s} v_L(\tau)d\tau$$

    where v_L = voltage across inductor; i = current through inductor; L = inductance; T_s = period of switching waveform.

    Because $i(t)$ is periodic, $\quad i(t+T_s) - i(t) = 0 \quad \rightarrow \quad \int_t^{t+T_s} v_L(\tau)d\tau = 0$
  - capacitor charge (ampere-second) balance

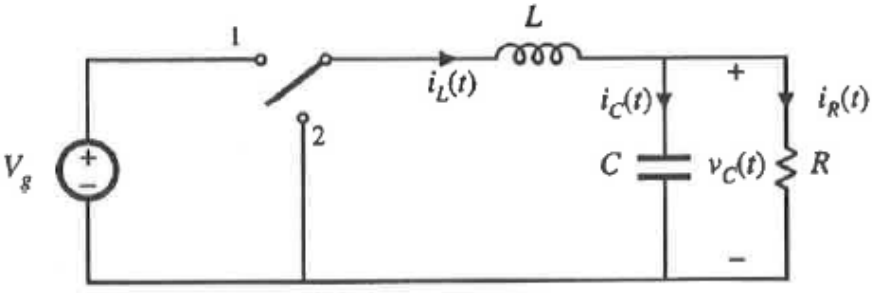
    $$i_C(t) = C\frac{dv(t)}{dt} \quad \rightarrow \quad v(t+T_s) - v(t) = \frac{1}{C}\int_t^{t+T_s} i_C(\tau)d\tau$$

    where v = voltage across capacitor; i_C = current through capacitor; C = capacitance; T_s = period of switching waveform.

    Because $v(t)$ is periodic, $\quad v(t+T_s) - v(t) = 0 \quad \rightarrow \quad \int_t^{t+T_s} i_C(\tau)d\tau = 0$
- switching waveform
  - D = duty cycle, where $0 < D < 1$; usually, duty cycle is fraction of switching waveform cycle during which the switching voltage is "high" (positive value); "low" switching voltage is usually zero.
  - switching voltage waveform could have constant D or variable D
  - D usually nominally constant in DC-to-DC converters but can vary slightly if feedback is used to stabilize output voltage
  - continuously variable D used in bridge-type DC-to-AC inverters, for example.
  - in practice, transistor does not switch cleanly; charge/discharge of gate-to-source and gate-to-drain capacitances can cause distortion of output voltage waveform beyond ripple on output filter capacitor; stray inductance and capacitance can combine to cause "ringing" (damped oscillations); sophisticated design and filtering methods are required to eliminate these types of transients

Buck converters

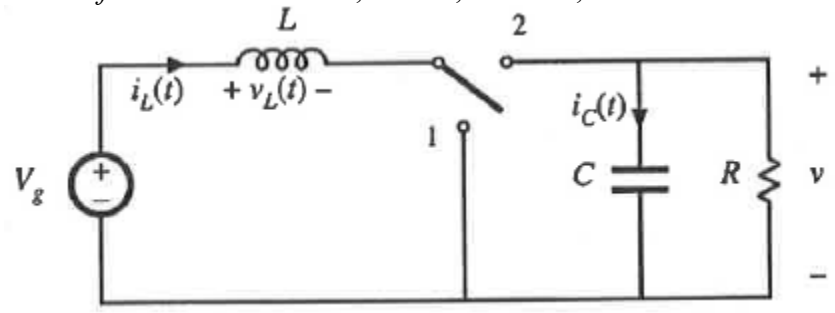
- conceptual circuit layout [diagram from R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed., Norwell, MA: Kluwer Academic, 2001.]



- design equations (assuming ideal components)
  - V = DC average output voltage; Δv = peak output voltage ripple; D = duty cycle (time switch is in position 1)
  - output voltage: $V = DV_g$
  - inductor current ripple: $\Delta i_L = \dfrac{(V_g - V)DT_s}{2L}$
  - capacitor voltage ripple: $\Delta v = \dfrac{\Delta i_L T_s}{8C}$

Boost converters

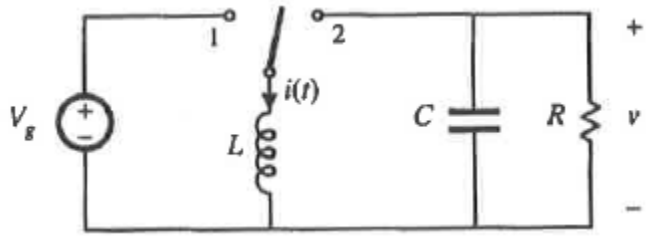
- conceptual circuit layout [diagram from R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed., Norwell, MA: Kluwer Academic, 2001.]



- design equations (assuming ideal components)
  - V = DC average output voltage; Δv = peak output voltage ripple; D = duty cycle (time switch is in position 1)
  - output voltage: $V = \dfrac{V_g}{1-D}$
  - inductor current ripple: $\Delta i_L = \dfrac{V_g D T_s}{2L}$
  - capacitor voltage ripple: $\Delta v = \dfrac{V D T_s}{2RC}$

Buck-boost (inverting) converters

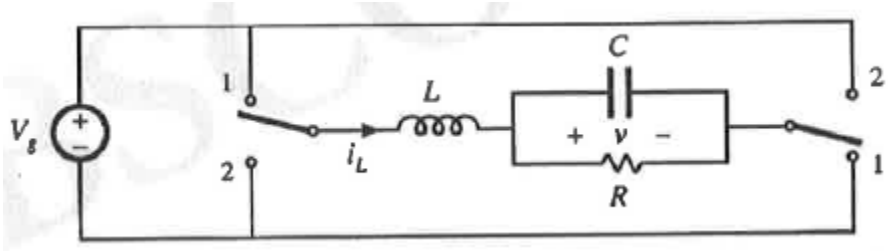
- conceptual circuit layout [diagram from R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed., Norwell, MA: Kluwer Academic, 2001.]



- design equations (assuming ideal components)
  - V = DC average output voltage (negative value); Δv = peak output voltage ripple; D = duty cycle (time switch is in position 1)
  - output voltage: $V = \dfrac{-V_g D}{1-D}$
  - inductor current ripple: $\Delta i = \dfrac{V_g D T_s}{2L}$
  - capacitor voltage ripple: $\Delta v = \dfrac{-V D T_s}{2RC}$

H-bridge converters

- conceptual circuit layout [diagram from R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, Norwell, MA: Kluwer Academic, 2001.]



- output voltage (assuming ideal components): $V = (2D-1)V_g$

  where V = DC average output voltage; D = duty cycle (time switch is in position 1)
- D can be made variable (with periodic variation) to produce AC

Effects of non-zero inductor resistance on switching regulator output voltage and efficiency

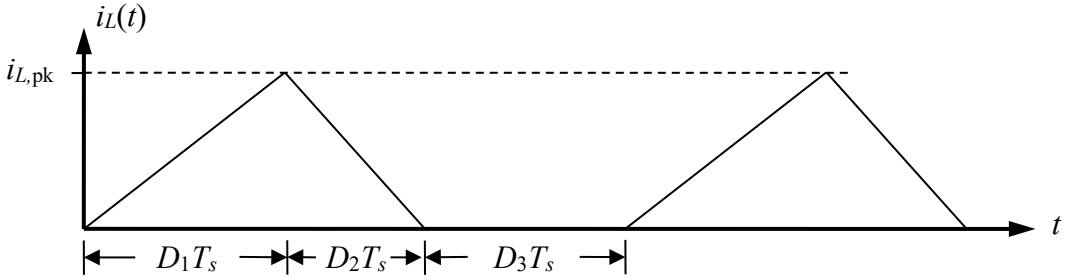
- R_L = inductor winding resistance; can be many ohms because windings tend to be numerous and use small-diameter wire
- R = load resistance
- D = duty cycle (time switch is in position 1); $D' = 1 - D$ (time in position 2)
- boost converter
  - output voltage: $V = \dfrac{V_g}{1-D} \dfrac{1}{1+\dfrac{R_L}{(1-D)^2 R}}$
  - efficiency: $\eta = \dfrac{1}{1+\dfrac{R_L}{(1-D)^2 R}}$
- buck-boost converter (voltage inverter)
  - output voltage: $V = \dfrac{-V_g D}{1-D} \dfrac{1}{1+\dfrac{R_L}{(1-D)^2 R}}$
  - efficiency: $\eta = \dfrac{1}{1+\dfrac{R_L}{(1-D)^2 R}}$

Other major sources of power loss and reduced output voltage in switching regulators

- diode forward voltage drop (Schottky diodes or MOSFETs preferred over standard diodes because they have lower voltage drop and switch quickly)
- diode on-resistance (included in diode voltage drop if load current is quasi-constant)
- on-resistance(s) of switching transistor(s)

DC-to-DC converters in discontinuous conduction mode (DCM)

- characterized by zero inductor current during part of the switching cycle
- typically occurs with large inductor current ripple and/or low load current
- voltage conversion ratio V/V_g is a more complicated function of multiple circuit parameters other than just duty cycle D; typically also includes inductor value, switching frequency (or period), and/or load current.
- inductor volt-second balance and capacitor charge (ampere-second) balance principles still apply



- in continuous conduction mode (CCM), $D_3 = 0$ because the inductor has nonzero current throughout the switching cycle
- at low output currents, D_3T_s can be very long compared to D_1T_s and D_2T_s because capacitor discharges slowly into load when diode is off (during D_1T_s and D_3T_s)
- for buck and boost converters, boundary between operation in CCM and DCM depends on relationship between duty cycle ($D = D_1$) and parameter K given by

  $K = \dfrac{2L}{RT_s}$, where L = inductor value, R = equiv. load resistance, T_s = switching period
- buck converters ($D = D_1$):

  $K_{crit} = 1 - D$

  $$\frac{V}{V_g} = \begin{cases} D & \text{for CCM, } K > K_{crit} \\ \dfrac{2}{1+\sqrt{1+\dfrac{4K}{D^2}}} & \text{for DCM, } K < K_{crit} \end{cases}$$
- boost converters ($D = D_1$):

  $K_{crit} = D(1 - D)^2$

  $$\frac{V}{V_g} = \begin{cases} \dfrac{1}{1-D} & \text{for CCM, } K > K_{crit} \\ \dfrac{1+\sqrt{1+\dfrac{4D^2}{K}}}{2} & \text{for DCM, } K < K_{crit} \end{cases}$$
- DCM analysis of boost converter:

  inductor volt-second balance leads to: $V = \dfrac{D_1 + D_2}{D_1} V_g$;

  capacitor charge balance leads to: $\dfrac{V_g D_1 D_2 T_s}{2L} = \dfrac{V}{R}$;

  combining them, eliminating D_2, and setting $D = D_1$ lead to: $V^2 - VV_g - \dfrac{V_g^2 D^2}{K} = 0$,

  which yields expression for V/V_g in DCM

- DCM analysis of buck converter:

  inductor volt-second balance leads to: $V = \dfrac{D_1}{D_1 + D_2} V_g$;

  capacitor charge balance leads to: $\dfrac{D_1 T_s}{2L}\left(D_1 + D_2\right)\left(V_g - V\right) = \dfrac{V}{R}$;

  combining them, eliminating D_2, and setting $D = D_1$ yields expression for V/V_g in DCM

Thermal management and heat sinks

- concept of thermal resistance θ (sometimes labeled R_θ)
- relationship between junction-to-ambient temperature gradient and dissipated power
  - $T_J - T_A = \theta_{JA} P_D$ (analogous to Ohm's law)
  - T_J = device junction temperature (°C)
  - T_A = ambient temperature (°C)
  - θ_{JA} = thermal resistance from junction to ambient (°C/W); sometimes specified on datasheets
  - ambient (surrounding) medium is usually air, but it can be oil or a coolant in some cases
  - P_D = power dissipated by device (W)
  - T_A can be significantly higher in a device enclosure than the temperature of the air outside the enclosure. T_A = 50 °C is often assumed as a conservative estimate.
- junction-ambient thermal resistance when heat sink is used
  - $\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$ (analogous to series resistance formula)
  - θ_{JC} = junction-to-case thermal resistance (usually specified on datasheets; much less than θ_{JA})
  - θ_{CS} = case-to-heat sink thermal resistance (usually due to mica or silicone insulator with or w/o thermally conductive paste; value typically under 1.0 °C/W, often well under); this resistance is sometimes further decomposed into case-to-washer resistance θ_{CW} and washer-to-sink resistance θ_{WS}
  - θ_{SA} = heat sink-to-ambient thermal resistance (most important spec of heat sink; can be lowered with forced-air or liquid cooling)
- dissipated power P_D in BJTs:
  - $P_D = V_{CE} I_C + V_{BE} I_B$,
    where V_{CE} = quiescent collector-emitter voltage; I_C = quiescent collector current; V_{BE} = quiescent base-emitter voltage; I_B = quiescent base current
  - good approximation for BJT in active region:
    $P_D \approx V_{CE} I_C$
  - power dissipated in base-emitter path, $V_{BE}I_B$, is often negligible (unless BJT operates in saturation region; then $V_{BE}I_B$ might be significant)
- dissipated power P_D in FETs:
  - $P_D = V_{DS} I_D$,
    where V_{DS} = quiescent drain-source voltage; I_D = quiescent drain current
  - no significant power dissipated in gate-source path in analog and low-speed switching or digital applications since DC gate current is essentially zero
  - if FET is used in high-frequency switching circuit or high-speed digital circuits, there could be significant power dissipation in gate-source and/or gate-drain paths due to transient currents flowing into/out of gate to charge/discharge internal capacitances. This is the primary source of heat generation in high-speed digital circuits.

Relevant course material:

HW: #9 and #10
Labs: #5
Reading: Assignments from Apr. 10 through Apr. 29, including the supplemental readings
Fundamentals of Power Electronics, Chaps. 1, 2, 3, and 5
Secs. 12.10.1 and 12.10.4 from Sedra & Smith, 7th ed.
Fairchild Semiconductor Application Note AN-4166 "Heat Sink Mounting Guide" (might be helpful)

This exam will focus primarily on course outcomes #6 and #7 (listed below) and related topics.

6. Understand the fundamental operating principles of basic switching regulator (DC-to-DC converter) circuits.
7. Select an appropriate heat sink for an electronic device.

The course outcomes are listed on the Course Policies and Information sheet, which was distributed at the beginning of the semester and is available on the Syllabus and Policies page at the course web site. The outcomes are also listed on the Course Description page. Note, however, that some topics not directly related to the course outcomes could be covered on the exam as well.