CSCI 315 Operating Systems Design
Fall 2016 - Prof. Felipe Perrone
Activity 17

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1) Consider a system which uses paging. Assume that the latency of RAM memory is Δ and derive an expression for the *effective access time* (EAT) to one memory location in this system.

2) Now, assume that we add to the processor in this system a *translation lookaside buffer* (TLB). Assuming that the latency to the TLB is τ and that the probability of a TLB hit is ϕ, derive the expression for the EAT in this improved system.

3) Using the expression that you derived above for the EAT with a TLB, determine the necessary condition (in terms of the parameters Δ, τ, and ϕ) for your *"improved"* system to exhibit EAT better than the original system.