ECEG 350 **Electronics I** **Fall 2023**

Policies and Review Topics for Exam #1

The following policies will be in effect for the exam. They will be included in a list of instructions and policies on the first page of the exam:

1. You will be allowed to use a non-wireless enabled calculator, such as a TI-99.
2. You will be allowed to use one 8.5 × 11-inch two-sided handwritten help sheet. No photocopied material or copied and pasted text or images are allowed. If there is a table or image from the textbook or some other source that you feel would be helpful during the exam, please notify me.
3. All help sheets will be collected at the end of the exam but will be returned to you later.
4. **You may not leave the exam room without prior permission except in an emergency or for an urgent medical condition. Please use the restroom before the exam.**

The following is a list of topics that could appear in one form or another on the exam. Not all of these topics will be covered, and it is possible that an exam problem could cover a detail not specifically listed here. However, this list has been made as comprehensive as possible.

Although significant effort has been made to ensure that there are no errors in this review sheet, some might nevertheless appear. The textbook is the final authority in all factual matters, unless errors have been specifically identified there. You are ultimately responsible for obtaining accurate information when preparing for the exam.

General amplifier concepts and background

- linear vs. nonlinear regions of operation
- concept of a signal; voltage and current signals
- concept of a circuit "port" (pair of terminals)
- concepts of signal sources and loads (TEC/NEC of a source includes a V or I source; TEC/NEC of a load contains no V or I source; both include equivalent resistance)

Background information on operational amplifiers

- op-amp equivalent circuit model (for ideal and non-ideal cases)
- op-amp output voltage limited by power supply voltages (saturation or clipping)
- basic inverting amplifier circuit
- basic noninverting amplifier circuit; voltage follower
- basic summing amplifier circuit
- ideal op-amp characteristics
    - infinite open-loop gain
    - infinite input resistance between input terminals
    - zero output resistance
    - zero current flow into the inverting and noninverting inputs
    - output voltage can swing all the way to the power supply voltages
    - no output current limit
- closed-loop voltage gain vs. open-loop voltage gain
- virtual short if neg. feedback is present and op-amp operates in linear region

- non-ideal characteristics
  - finite open-loop gain, non-zero voltage across op-amp's input terminals; it is very small if neg. feedback is present (almost always ignored)
  - finite input resistance between input terminals (almost always ignored)
  - non-zero output resistance (almost always ignored)
  - output voltage swing cannot reach power supply voltages
  - output current limiting
  - input offset voltage
  - input bias currents
  - slew rate limiting (not covered on this exam)
  - bandwidth limit (not covered on this exam)
- effects of negative feedback
  - only present if output voltage is free to react to circuit changes (not possible if voltage/current/slew rate limiting occurs)
  - offsets the effect of any variation in the open-loop gain and some other parameters
  - produces virtual short between input terminals
  - reduces effective output impedance of op-amp output port
  - increases effective input impedance between op-amp's input terminals

DC imperfections of op-amps

- input offset voltage
  - DC effect (i.e., not time varying)
  - model using ideal voltage source V_{OS} in series with either non-inverting or inverting input of op-amp
  - polarity of V_{OS} varies from op-amp to op-amp (unpredictable)
  - how to determine component of output voltage due to V_{OS} (use superposition)
  - can use offset null potentiometer to mitigate effects if available on chip; other circuits can be used if offset null terminals are not available
- input bias currents
  - DC effect (i.e., not time varying)
  - model using ideal current sources I_{B1} and I_{B2} at op-amp's input terminals
  - currents I_{B1} and I_{B2} always flow *into* op-amp terminals (except possibly for rare special cases; one such case is an op-amp with PNP-type BJTs at inputs)
  - datasheets give average input bias current: $I_B = 0.5(I_{B1} + I_{B2})$, that is, the average of I_{B1} and I_{B2}
  - datasheets sometimes give input offset current, defined as $I_{OS} = |I_{B1} - I_{B2}|$
  - unequal bias currents can be expressed as $I_{B1} = I_B \pm 0.5I_{OS}$ and $I_{B2} = I_B \mp 0.5I_{OS}$ ($0.5I_{OS}$ adds to one and subtracts from other; either I_{B1} or I_{B2} could be larger)
  - can sometimes mitigate effects of average bias current (I_B) using a resistor in series with the non-inverting input (e.g., R_3 in Fig. 2.35 of Sedra & Smith, 8th ed.)
  - can mitigate effects of input offset current I_{OS} using offset null potentiometer, as with V_{OS} (I_{OS} and V_{OS} might partially cancel each other in some cases)
  - how to determine component of output voltage due to I_{B1} and I_{B2} (superposition)
  - I_{B1} and I_{B2} can cause unintended charging of capacitors connected to op-amp if an alternative path for DC is not available. Current-voltage relationship for capacitors:

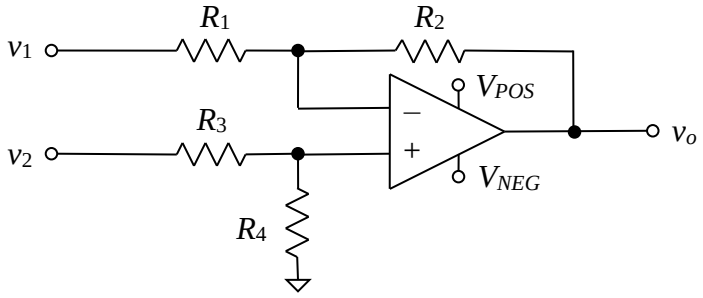
    $i_C = C\frac{dv_C}{dt}$, where i_C flows from positive side of v_C to negative side

- can mitigate all three DC imperfections (V_{OS}, I_{B1}, I_{B2}) simultaneously through proper use of a DC voltage source added to circuit and/or additional resistors; can also mitigate using offset null potentiometer if terminals are available on chip

Differential signaling

- used in USB, Ethernet, balanced audio (most XLR connectors), RS-422, RS-485, HDMI, and many other signal transmission standards
- in single-ended (not differential) systems, an input/output port has one terminal grounded
- in single-ended systems, signal detection problems can occur with physically separated local grounds between the sensor and the amplifier (i.e., widely separated "ground" connections can have significant noise/interference voltage drops between them)
- concept of floating terminals (floating means that neither terminal is grounded)
- voltage signal from sensor or other signal source is applied *between* the two conductors in the cable (transmission line) that connects the source to the amplifier's input, so it is called a differential-mode voltage (or current)
- many types of electronic noise and interference (undesired signals) appear on both conductors of the cable in equal amounts relative to ground, so they are called common-mode voltages (or currents); they can be suppressed using a difference amp
- IF the majority of the incoming noise in a system is of the common-mode type, then the signal-to-noise ratio (SNR) can be improved by a factor equal to the common-mode rejection ratio (CMRR) of a difference amplifier. Note that this is only true if most of the noise is external to the system and of the common-mode type. In most radio/wireless systems, the most significant noise is differential-mode and/or it is generated within the amplifying transistor(s). In the latter case, the SNR degrades between the input and output ports of an amplifier.

Difference amplifier (a.k.a. differential amplifier) based on op-amp



- has "floating" inputs; i.e., neither v_1 nor v_2 is normally connected to ground node
- differential vs. single-ended input/output ports
  - differential inputs/outputs are both floating
  - single-ended inputs/outputs have one terminal grounded
- purposes/advantages of difference amplifiers
- differential-mode vs. common-mode signals

  $v_{Id} = v_2 - v_1$ and $v_{Icm} = \frac{v_2 + v_1}{2}$,

  where v_{Id} = differential-mode input voltage; v_{Icm} = common-mode input voltage
- decomposition of single-ended input voltages (v_1 and v_2) into differential and common-mode input voltages v_{Id} and v_{Icm} (i.e., two types of voltages are simultaneously present at each input terminal; can think of it as another application of superposition)

  $v_1 = v_{Icm} - 0.5v_{Id}$ and $v_2 = v_{Icm} + 0.5v_{Id}$

- total (differential-mode plus common-mode) output voltage

  $v_o = \frac{1}{2}\left[\left(1+\frac{R_2}{R_1}\right)\left(\frac{R_4}{R_3+R_4}\right)+\frac{R_2}{R_1}\right]v_{Id} + \left[\left(1+\frac{R_2}{R_1}\right)\frac{R_4}{R_3+R_4}-\frac{R_2}{R_1}\right]v_{Icm}$, or

  $v_o = \frac{1}{2}\left[\left(1+\frac{R_2}{R_1}\right)\left(\frac{R_4}{R_3+R_4}\right)+\frac{R_2}{R_1}\right]v_{Id} + \frac{R_4}{R_3+R_4}\left(1-\frac{R_2}{R_1}\frac{R_3}{R_4}\right)v_{Icm}$ (alternative)

- differential-mode gain vs. common-mode gain

  $v_o = v_{od} + v_{ocm} = A_d v_{Id} + A_{cm} v_{Icm}$, where

  $A_d = \frac{v_{od}}{v_{Id}} = \frac{1}{2}\left[\left(1+\frac{R_2}{R_1}\right)\left(\frac{R_4}{R_3+R_4}\right)+\frac{R_2}{R_1}\right]$

  $A_{cm} = \frac{v_{ocm}}{v_{Icm}} = \left(1+\frac{R_2}{R_1}\right)\frac{R_4}{R_3+R_4}-\frac{R_2}{R_1} = \frac{R_4}{R_3+R_4}\left(1-\frac{R_2}{R_1}\frac{R_3}{R_4}\right)$

- if $R_4/R_3 = R_2/R_1$ (exact match), then $A_d = R_2/R_1$ and $A_{cm} = 0$
- if $R_4/R_3 \approx R_2/R_1$ (approximate match), then $A_d \approx R_2/R_1$ and A_{cm} is very small (<< 1):

  $A_{cm} \approx \pm 4\varepsilon \frac{R_4}{R_3+R_4} = \pm 4\varepsilon \frac{R_4/R_3}{1+R_4/R_3} \approx \pm 4\varepsilon \frac{A_d}{1+A_d}$; the algebraic sign (±) depends on whether R_4/R_3 is greater than or less than R_2/R_1

- note that only the resistor *ratios* have to match (or nearly match) for A_{cm} to be zero (or small), but setting $R_1 \approx R_3$ and $R_2 \approx R_4$ helps to mitigate effect of input bias currents
- differential-mode input resistance between input ports: $R_{id} = R_1 + R_3$; this is roughly equal to $2R_1$ if $R_1 \approx R_3$.
- common mode rejection ratio (CMRR)

  $\text{CMRR} = \left|\frac{A_d}{A_{cm}}\right|$

- Worst-case CMRR quantifies maximum possible performance degradation due to resistor tolerance (the lower the CMRR, the more the common-mode signal intrudes on the differential-mode signal at the amplifier's output):

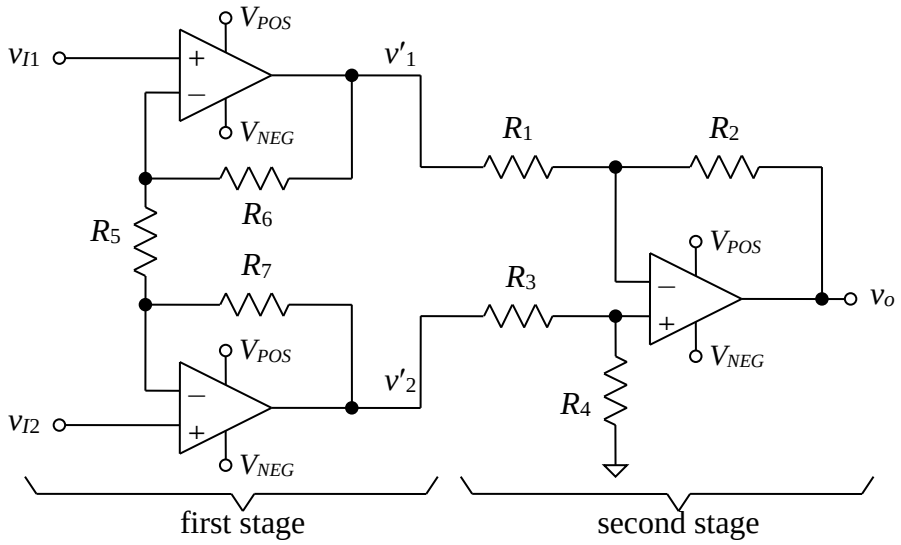
  $\text{CMRR}_{\min} = \frac{1+A_d}{4\varepsilon}$,

  where ε = fractional tolerance of resistors (e.g., for 5% resistors, $\varepsilon = 0.05$) and A_d is the nominal differential-mode gain (equals R_2/R_1 in circuit shown above)
- CMRR is usually expressed in dB: CMRR [dB] = 20 log(CMRR), where "log" is the common (base 10) logarithm
- dB form-to-ratio form conversion: $\text{CMRR} = 10^{\text{CMRR [dB]}/20}$
- don't confuse CMRR in ratio form with CMRR expressed in dB

Decibel and decibel-based units

- definition; advantage over using voltage and power ratios
- application to voltage gain vs. power gain
- in terms of *V* gain: $\text{G [dB]} = 20\log\left(\frac{V_{out}}{V_{in}}\right)$; in terms of *P* gain: $\text{G [dB]} = 10\log\left(\frac{P_{out}}{P_{in}}\right)$
- overall gain/loss of a system in dB is equal to sum of gains/losses in dB of each stage
- mathematical identities involving logarithms

Instrumentation amplifier



- differential-mode gain of first stage can be controlled by varying a single resistor value (R_5 in diagram above)

  $$A_{d1} \approx 1 + \frac{R_6}{0.5R_5} \approx 1 + \frac{R_7}{0.5R_5}, \quad \text{where } R_7 \approx R_6$$

- common-mode signals are not amplified by first stage because common-mode gain of first stage is unity (acts like a voltage follower for cm signals)

  $$A_{cm1} = 1$$

  This is true only because R_5 is "floating." If middle of R_5 is connected to ground, then

  $$A_{cm1} \approx 1 + \frac{R_6}{0.5R_5} \approx 1 + \frac{R_7}{0.5R_5} \approx A_{d1}$$

- overall CMRR for instrumentation amp (if R_5 is floating):

  $$\text{CMRR}_{\text{total}} = \frac{|A_{d1}|}{|A_{cm1}|} \cdot \frac{|A_{d2}|}{|A_{cm2}|} = |A_{d1}| \frac{|A_{d2}|}{|A_{cm2}|} = |A_{d1}| \cdot \text{CMRR}_2 \quad \text{because } A_{cm1} = 1,$$

  where A_{d1} = diff-mode gain of 1st stage, A_{cm1} = common-mode gain of 1st stage, A_{d2} = diff-mode gain of 2nd stage, A_{cm2} = common-mode gain of 2nd stage
- worst-case CMRR for instrumentation amp (if R_5 is floating):

  $$\text{CMRR}_{\text{min}} = A_{d1} \frac{1 + A_{d2}}{4\varepsilon_2},$$

  where ε_2 = fractional resistor tolerance of 2nd stage
- resistor tolerance of 1st stage has negligible impact on overall CMRR (if R_5 is floating)
- differential-mode input resistance of instrumentation amp is very high (in the gigaohm range, much higher than for basic diff amp); this is a major advantage
- resistor values do not have to be matched closely in 1st stage for circuit to be effective; very high CMRR can be achieved using resistors with moderately loose tolerances in 1st stage. Common-mode rejection is achieved primarily in the 2nd stage; that stage is where it is best to apply tight-tolerance resistors.
- Common-mode rejection in the "inferior" instrumentation amplifier with R_5 split into halves and the middle node grounded (unlike the circuit above) is poor to nonexistent. Common-mode signals can actually be amplified in that case because they are partially converted to differential-mode signals due to R_6 and R_7 not being perfectly matched.

Relevant course material:

HW:	#1 through #4
Labs:	#1 and #2
Reading:	Assignments from Aug. 21 through Sept. 20, including the lecture notes: "Negative Feedback in the Op-Amp Inverter" "Grounding, Differential-Mode Signals, and Interference Rejection" (background) "Real-World Performance of Difference Amplifiers" "Why Do Engineers Use the Decibel Unit?"

This exam will focus primarily on the course outcomes listed below and related topics:

1. Predict and/or mitigate the effects of the nonideal properties of operational amplifiers on circuit performance. [except slew rate limiting]
2. Predict the common-mode and differential-mode performance of difference and instrumentation amplifiers based on operational amplifiers.

The course outcomes are listed on the Course Policies and Information sheet, which was distributed at the beginning of the semester and is available on the Syllabus and Policies page at the course web site. The outcomes are also listed on the Course Description page. Note, however, that some topics not directly related to the course outcomes could be covered on the exam as well.