

Policies and Review Topics for Exam #2

The following policies will be in effect for the exam. They will be included in a list of instructions and policies on the first page of the exam:

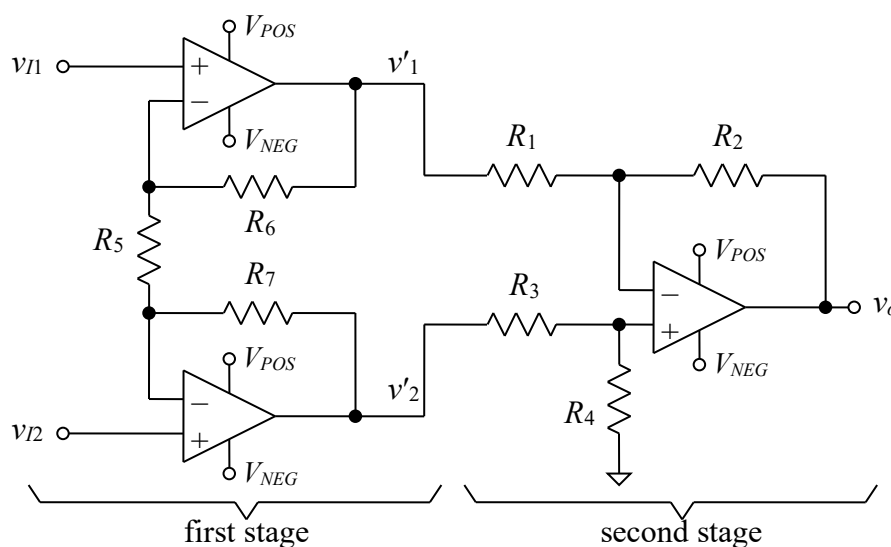
1. You will be allowed to use a non-wireless enabled calculator, such as a TI-99.
2. You will be allowed to use two 8.5×11 -inch two-sided handwritten help sheets. No photocopied material or copied and pasted text or images are allowed. If there is a table or image from the textbook or some other source that you feel would be helpful during the exam, please notify me.
3. All help sheets will be collected at the end of the exam but will be returned to you either immediately or soon after the exam.
4. Use of a help sheet that is not completely handwritten will result in an automatic 5-point score reduction.
5. If you begin the exam after the start time, you must complete it in the remaining allotted time. However, you may not take the exam if you arrive after the first student has completed it and left the room. The latter case is equivalent to missing the exam.
6. **You may not leave the exam room without prior permission except in an emergency or for an urgent medical condition. Please use the restroom before the exam.**

The exam will take place 8:00–9:50 am on Thursday, October 23 in Breakiron 066.

The following is a list of topics that could appear in one form or another on the exam. Not all of these topics will be covered, and it is possible that an exam problem could cover a detail not specifically listed here. However, this list has been made as comprehensive as possible. You should be familiar with the topics on the previous review sheet in addition to those listed below.

Although significant effort has been made to ensure that there are no errors in this review sheet, some might nevertheless appear. The textbook and the supplemental readings are the final authority in all factual matters, unless errors have been specifically identified there. You are ultimately responsible for obtaining accurate information when preparing for the exam.

Instrumentation amplifier



- differential-mode gain of first stage can be controlled by varying a single resistor value (R_5 in diagram above)

$$A_{d1} \approx 1 + \frac{2R_6}{R_5} \approx 1 + \frac{2R_7}{R_5}, \quad \text{where } R_7 \approx R_6$$

- common-mode signals are not amplified by first stage because common-mode gain of first stage is unity (acts like a voltage follower for cm signals)

$$A_{cm1} = 1$$

This is true only because R_5 is “floating.” If middle of R_5 is connected to ground, then

$$A_{cm1} \approx 1 + \frac{2R_6}{R_5} \approx 1 + \frac{2R_7}{R_5} \approx A_{d1}$$

- overall CMRR for instrumentation amp (if R_5 is floating):

$$\text{CMRR}_{\text{total}} = \frac{|A_{d1}|}{|A_{cm1}|} \cdot \frac{|A_{d2}|}{|A_{cm2}|} = |A_{d1}| \frac{|A_{d2}|}{|A_{cm2}|} = |A_{d1}| \cdot \text{CMRR}_2 \quad \text{because } A_{cm1} = 1,$$

where A_{d1} = diff-mode gain of 1st stage, A_{cm1} = common-mode gain of 1st stage, A_{d2} = diff-mode gain of 2nd stage, A_{cm2} = common-mode gain of 2nd stage

- worst-case CMRR for instrumentation amp (if R_5 is floating):

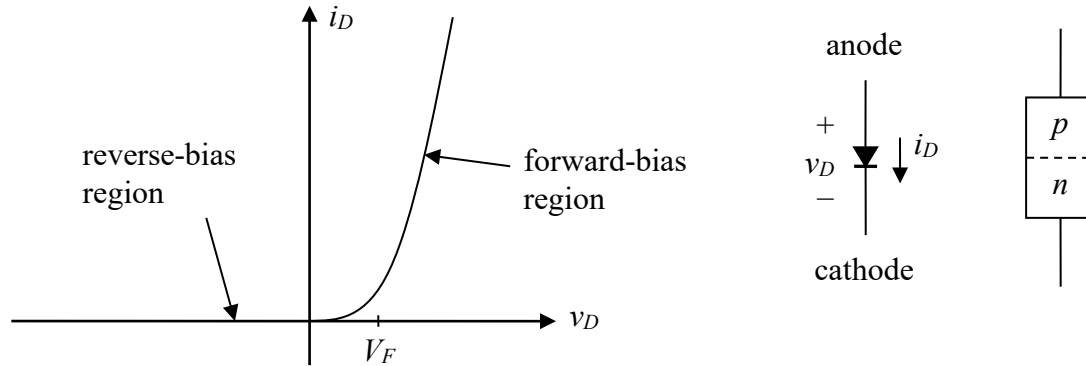
$$\text{CMRR}_{\text{min}} = A_{d1} \frac{1 + A_{d2}}{4\varepsilon_2},$$

where ε_2 = fractional resistor tolerance of 2nd stage

- resistor tolerance of 1st stage has negligible impact on overall CMRR (if R_5 is floating)
- differential-mode input resistance of instrumentation amp is very high (in the gigaohm range, much higher than for basic diff amp); this is a major advantage
- resistor values do not have to be matched closely in 1st stage for circuit to be effective; very high CMRR can be achieved using resistors with moderately loose tolerances in 1st stage. Common-mode rejection is achieved primarily in the 2nd stage; that stage is where it is best to apply tight-tolerance resistors.
- Common-mode rejection in the amplifier with R_5 split into halves and the node between them grounded (unlike the circuit above) is poor to nonexistent. Common-mode signals can actually be amplified in that circuit because they are partially converted to differential-mode signals due to R_6 and R_7 not being perfectly matched.

Semiconductors based on silicon (Si)

- holes and electrons
- acceptor and donor impurities (group III and V elements on the periodic chart)
- n -type vs. p -type material
- free charges vs. immobile charges (latter are ions locked in crystal structure)
- depletion region and the built-in field
- diffusion current vs. drift current

pn-junction diode operation

- in the symbol, the bar and the forward sides of the arrow form a “K” for “kathode”
- basic construction; doping of pure silicon with Group III and V elements
- diode symbol and correct orientation
- reverse bias enhances built-in electric field across depletion region and therefore prevents current flow via diffusion; force of electric field exceeds diffusion “force”
- forward bias suppresses built-in electric field across depletion region and therefore allows current to flow, primarily through diffusion of holes and electrons; diffusion “force” overcomes force of built-in electric field
- i - v characteristic and orientation of i_D and v_D relative to diode symbol
- graphical and iterative analyses of diode circuits (load lines and/or transcendental equations)
- diode equation: $i_D = I_S \left(e^{v_D/\eta V_T} - 1 \right)$,

where I_S = scale or saturation current, η = emission coefficient, and V_T = thermal voltage

$$V_T = \frac{T}{11,600}, \text{ where } T = \text{temperature in kelvins}$$

I_S is very small (10^{-15} to 10^{-8} A) but proportional to junction area and highly dependent on temperature

$\eta = 1$ to 2 for most Si diodes (different values for other types); empirically determined values of η and V_F are very different for light-emitting diodes (LEDs) and depend on color; differences are primarily due to presence of large quantities of other elements besides silicon in the construction of the diode

Piecewise linear (PWL) diode models (applicable to *pn*-junction and zener types)

- turn-on (V_F) voltage
- diode behavior along different segments of PWL i - v characteristic
- [not on exam, but good to know:] forward (r_d) and zener (r_Z) resistances
- [not on exam, but good to know:] dependence of forward resistance on avg. (DC) diode current:

$$r_d = \frac{\eta V_T}{i_D} \approx \frac{\eta V_T}{I_D},$$

where i_D = total diode current (AC + DC); I_D = quiescent diode current (DC component only)

Constant-voltage diode model (special case of the piecewise linear diode model)

- simplest PWL model other than ideal model & adequate for most analyses
- ideal diode model is the constant-voltage model with $V_F = 0$
- ON state: diode acts like voltage source; $v_D = V_F$ (behavior) and $i_D > 0$ (check)
- OFF state: diode acts like an open; $i_D = 0$ (behavior) and $v_D < V_F$ (check)
- for analysis, assume state of each diode, which dictates its behavior, and perform normal linear circuit analysis. Then verify (check) each assumed diode state. If validity of assumption is confirmed, then analysis is done; if not, then one or more diodes are in the opposite state.

Rectifier circuits

- half-wave rectifiers
- full-wave rectifiers (bridge and with center-tapped transformer)
- pulsating DC and its average value
- effect of diode voltage drop(s) on output voltage of rectifier
- diode on/off states change over period of AC waveform
- relationships between frequency (f), radian frequency (ω), and period (T) of AC waveforms
- transformer secondary voltage selection; understand differences b/w pk, rms, and peak-to-peak (pp) voltages and how to convert between them
- full secondary voltage vs. voltages between ends of winding and center-tap
- peak reverse (inverse) voltage and PRV (or PIV) ratings of diodes – max. safe reverse bias voltage that can be applied
- effects of diode failures (when failed diodes act as open circuits)

Power supply ripple filters

- filter capacitor selection vs. equiv. load resistance and/or load current (V_P = peak value of output voltage, V_r = ripple voltage), and derivation of formulas:

$$C_{\min} \approx \frac{1}{f R_{L\min} (V_r/V_P)} \approx \frac{i_{L\max}}{f V_r} \text{ (half-wave rectifier)}$$

$$C_{\min} \approx \frac{1}{2f R_{L\min} (V_r/V_P)} \approx \frac{i_{L\max}}{2f V_r} \text{ (full-wave rectifier, center-tapped or bridge)}$$

$$\text{based on } i_c = C \frac{dv_c}{dt} \approx -C \frac{V_r}{0.5T} \text{ (full-wave rectifier) or } -C \frac{V_r}{T} \text{ (half-wave rectifier),}$$

where i_c , v_c = capacitor current and voltage; T, f = period and frequency of AC waveform

- electrolytic capacitors can have very loose tolerances (up to 40% or more)
- ripple voltage, percentage ripple, and fractional ripple
- interpretation of $i_{L\max}$ in $C_{\min}$ formula; it represents *all* of the current that the capacitor must supply during its discharge interval; the “L” in the subscript of $i_{L\max}$ refers to the load on the capacitor, not just the load on the power supply (power supply’s load might be a subset of capacitor’s load)
- selection of bleeder resistor for filter capacitor
- peak diode current:

$$i_{D\max} = I_L \left(1 + 2\pi \sqrt{2V_{\text{sec,pk}}/V_r} \right) \text{ (half-wave rectifier)}$$

$$i_{D\max} = I_L \left(1 + 2\pi \sqrt{V_{\text{sec,pk}}/2V_r} \right) \text{ (full-wave rectifier)}$$

where $V_{\text{sec,pk}}$ = peak value of transformer’s secondary winding voltage for half-wave and full-wave bridge rectifiers or peak value of secondary half-voltage for full-wave rectifier with center tap; V_r = ripple voltage

- average diode current (averaged only over the conduction interval):

$$i_{Dav} = I_L \left(1 + \pi \sqrt{2V_{\text{sec,pk}}/V_r} \right) \text{ (half-wave rectifier)}$$

$$i_{Dav} = I_L \left(1 + \pi \sqrt{V_{\text{sec,pk}}/2V_r} \right) \text{ (full-wave rectifier)}$$

- individual diode conduction time (for both half and full-wave rectifiers)

$$\Delta t = \frac{1}{\omega} \sqrt{\frac{2V_r}{V_{\text{sec,pk}}}} = \frac{1}{2\pi f} \sqrt{\frac{2V_r}{V_{\text{sec,pk}}}} = \frac{T}{2\pi} \sqrt{\frac{2V_r}{V_{\text{sec,pk}}}},$$

where $V_{\text{sec,pk}}$ and V_r have the same definitions as above

Relevant course material:

HW: #3 and #4

Labs: #3

Readings: Assignments from Sept. 17 through Oct. 10 (except Sec. 2.8.3 and the supplemental reading “Three-Terminal Linear Voltage Regulators”), including the lecture notes:

“Why Do Engineers Use the Decibel Unit?”

“Average and Peak Diode Currents in Rectifier Circuits”

This exam will focus primarily on the course outcomes listed below and related topics:

2. Predict the common-mode and differential-mode performance of difference and instrumentation amplifiers based on operational amplifiers. [instrumentation amplifiers only]
3. Analyze and/or design circuits involving diodes using the piecewise linear diode model.
4. Analyze and/or design power supply circuits using linear voltage regulators. [only basic rectifier/filter power supply circuits without linear voltage regulators]

The course outcomes are listed on the Course Policies and Information sheet, which was distributed at the beginning of the semester and is available on the Syllabus and Policies page at the course web site. The outcomes are also listed on the Course Description page. Note, however, that some topics not directly related to the course outcomes could be covered on the exam as well.