**ECEG 350** **Electronics I** **Fall 2023**

**Homework Assignment #2 – due via Moodle at 11:59 pm on Friday, Sept. 8, 2023**
**[revised 9/4/23 and 9/7/23; Graded Probs. 2 and 5 deferred to HW #3]**

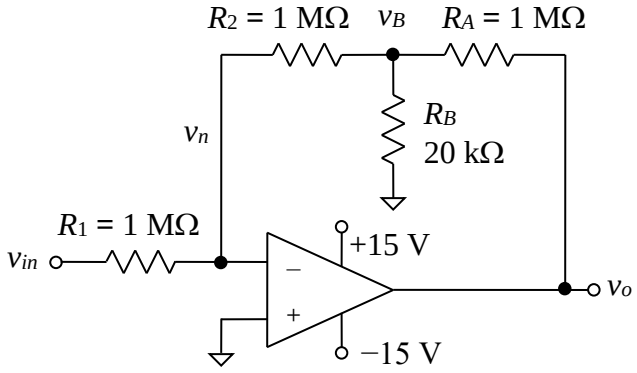
***Instructions, notes, and hints*:**

You may make reasonable assumptions and approximations in order to compensate for missing information, if any. Provide the details of all solutions, including important intermediate steps. You will not receive credit if you do not show your work.

Note that the first few problems will be graded and the rest will not be graded. Only the graded problems must be submitted by the deadline above; do not submit the ungraded problems.

***Graded Problems:***

1. The inverting amplifier shown below uses a T-network to obtain a closed-loop voltage gain of $v_o/v_{in} = -52$ V/V. As we saw in the previous homework set, these types of amplifiers exacerbate the effect of the input offset voltage $V_{OS}$. They do the same thing with the input bias currents. Suppose that the op-amp below has $I_{B1} = 75$ nA (into the inverting terminal) and $I_{B2} = 85$ nA. Find the output voltages due to $I_{B1}$ and $I_{B2}$ when the input signal voltage is zero (i.e., $v_{in} = 0$). You may ignore the effects of the finite open-loop gain and the input offset voltage.




2. **[deferred to HW #3]** Suppose that you have been asked to design a new digital data link, and the system needs a basic diff amp like the one shown in Figure 2.16 in the textbook (Sedra & Smith, 8th ed.). The differential-mode gain must be around 20 V/V, and the differential-mode input resistance must be $R_{id} = 50$ kΩ. The power supply voltages are to be ±10 V. The selected op-amp has a maximum rated output current of 30 mA, a maximum input bias current of 20 nA, and a peak input offset voltage magnitude of 1.5 mV. Find the maximum allowable tolerance for the resistors $R_1$ through $R_4$ to ensure that the CMRR of the diff amp would be at least 75 dB.

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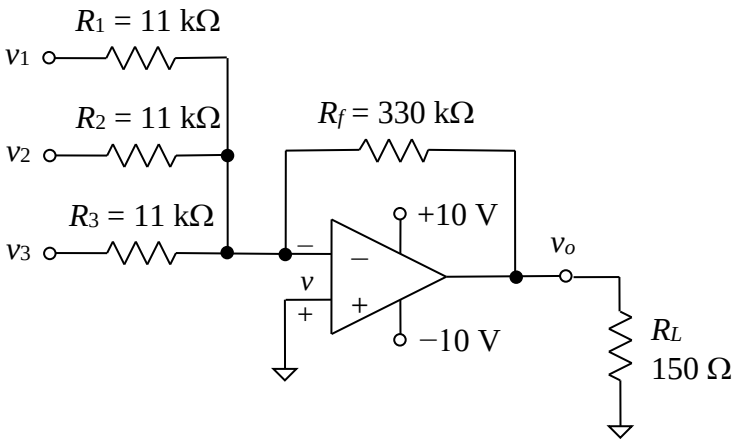
3. An LM741C op-amp is used in the summing amplifier shown below. The output voltage $v_o$ can swing to ±8.5 V. The output is connected to a recording device that has an input resistance of 150 Ω, which acts like a 150 Ω load on the summing amp. Input terminals $v_1$ through $v_3$ are connected to pressure sensors that can be modeled as ideal voltage sources. The first two sensors are exposed to constant pressures and produce DC output voltages of $v_1$ = 15 mV and $v_2$ = 24 mV. The third sensor is exposed to an exponentially increasing voltage that starts at $v_3(0)$ = 0 V and approaches 120 mV after a long period of time according to the expression for $v_3$ given below. Find the moment in time at which the op-amp experiences output current limiting, and find the corresponding output voltage $v_o$. Also find the value of the voltage $v$ across the op-amp's input terminals after $v_3$ has stabilized at its final voltage. You will need to consult the LM741C op-amp datasheet (available on the Laboratory page at the course web site) to obtain the typical value of the output current limit.




$$v_3(t) = 0.120\left(1 - e^{-0.125t}\right) \text{ V},$$

for t > 0.

4. Now suppose that the recording device connected to the output of the summing amplifier in the previous problem is replaced with a new one with an equivalent input resistance of 800 kΩ. It is so high that output current limiting is no longer a concern. However, the output voltage of the sensor connected to terminal $v_1$ rises to 450 mV. Determine whether the op-amp experiences output voltage clipping after voltage $v_3$ reaches its maximum value and, if so, find the value of voltage $v$ between the input terminals. All of the other circuit quantities and op-amp properties are the same as in the previous problem.

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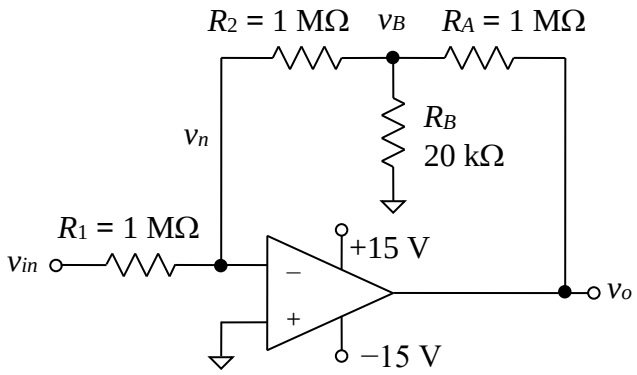
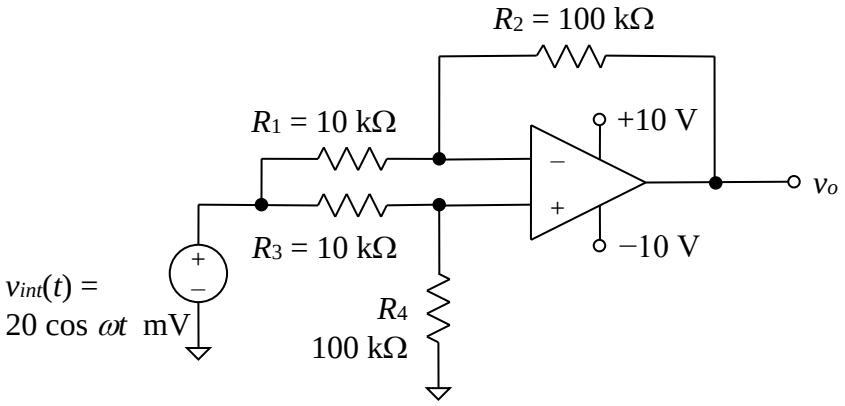
***Ungraded Problems*:**

The following problems will not be graded. They are intended to serve as practice problems and examples. The solutions will be posted along with the solutions to the graded problems. You should attempt to solve them on your own and then check the solutions afterwards. Do not give up too quickly if you struggle with any of them. Move on to a different problem and then come back to the difficult one after a few hours.

1. For the amplifier shown below, assume that the input bias currents of the op-amp are unknown but that $I_{B1} \approx I_{B2}$. To mitigate the effect of the input bias currents on the output voltage, a resistor $R_x$ will be inserted in series with the noninverting input terminal of the op-amp. Find the required value of resistor $R_x$.




2. The circuit shown below models a diff amp that has its input terminals shorted together so that the differential-mode input voltage is zero. However, the diff amp does experience a common-mode interference signal $v_{int}(t)$ at its inputs. The interference frequency is $f$ = 100 kHz. Nominal resistor values are shown, but the resistor tolerance is 5%. Assuming that the actual resistor values are no more than ±5% away from their respective nominal values, find the worst-case magnitude of the common-mode output voltage $v_o$.

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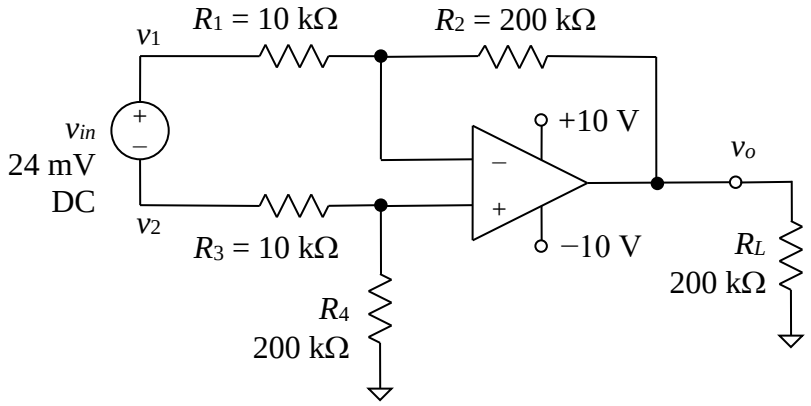
3. The resistors in the diff amp circuit diagram below are labeled with their nominal (ideal) values. Each one has a 2% tolerance. The actual resistor values (to four-digit accuracy) are $R_1$ = 10.10 kΩ, $R_2$ = 196.4 kΩ, $R_3$ = 10.14 kΩ, and $R_4$ =198.8 kΩ. The input voltage is quasi-DC (i.e., very slowly varying) and currently has a value of 24 mV. Although not shown in the diagram, the sensor generating the input voltage is connected to the amplifier using a very long cable in a noisy environment. The strongest noise source is the building's AC wiring, and it causes a common-mode input voltage expressed as $v_{Icm}(t)$ = 0.140 cos(377$t$) V to appear at each input of the amplifier. Note that $|v_{in}| < |v_{Icm}|_{pk}$. Find:

    a. the nominal differential-mode gain (i.e., the gain assuming ideal resistor values).
    b. the actual differential-mode gain $A_d$ (using actual resistor values).
    c. the actual common-mode gain $A_{cm}$.
    d. the actual CMRR (in dB).
    e. the differential-mode output voltage $v_{od}$.
    f. the common-mode output voltage $v_{ocm}$.




4. Suppose that the resistors in the diff amp in the previous problem are replaced with new resistors that have 5% tolerance. The actual resistor values are now $R_1$ = 10.42 kΩ, $R_2$ = 191.0 kΩ, $R_3$ = 10.38 kΩ, and $R_4$ = 205.6 kΩ. Repeat parts a through f of the previous problem. Comment on the relative changes in the differential-mode gain and the common-mode gain.

5. In the circuit shown on the next page, the op-amp is not ideal and has input bias currents of roughly 80 nA flowing into each terminal (i.e., $I_{B1} \approx I_{B2}$). Find the approximate output voltage $v_o$ (to two digits of accuracy since the resistor values are given to only two digits) due only to the two input bias currents (i.e., for the case $v_1 = v_2 = V_{OS} = 0$) for the following two sets of values for resistors $R_3$ and $R_4$, and explain the significance of the results. The resistor tolerances are 0.1%. Note that the differential-mode gain is the same (15 V/V) for both parts; although $R_3$ and $R_4$ in part b do not have the same nominal values as $R_1$ and $R_2$, their ratio is the same.

    a. $R_3$ = 200 kΩ and $R_4$ = 3.0 MΩ (same as $R_1$ and $R_2$)
    b. $R_3$ = 10 kΩ and $R_4$ = 150 kΩ (same ratio as $R_2/R_1$)

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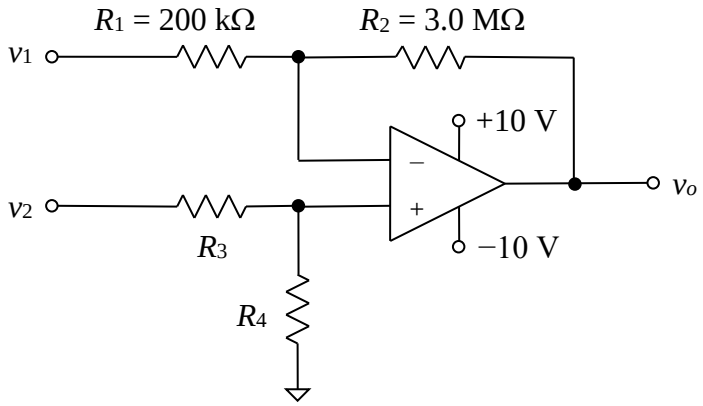


**Circuit diagram for UG Prob. 5.**

6. The input signal $v_{in}$ supplied to the amplifier circuit shown below is an AC voltage that can be expressed as $v_{in}(t) = V_m \cos(32{,}000\pi t - 60°)$ V, where $V_m$ is the amplitude of the voltage. Find the maximum value that $V_m$ can have to avoid clipping of the output voltage $v_o$. Assume that the actual output voltage limits are +8.5 V and −8.0 V. You may ignore the effects of the input offset voltage and input bias currents since they will be negligible in this case.