**ECEG 350 Electronics I Fall 2023**

**Homework Assignment #3 – due via Moodle at 11:59 pm on Friday, Sept. 15, 2023**
**[revised 9/14/23; Graded Probs. 5 and 6 deferred to HW #4]**

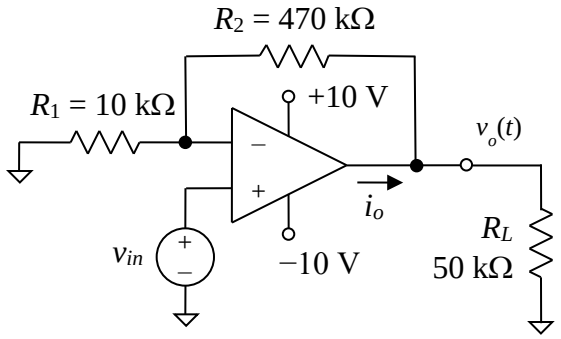
***Instructions, notes, and hints*:**

You may make reasonable assumptions and approximations in order to compensate for missing information, if any. Provide the details of all solutions, including important intermediate steps. You will not receive credit if you do not show your work.

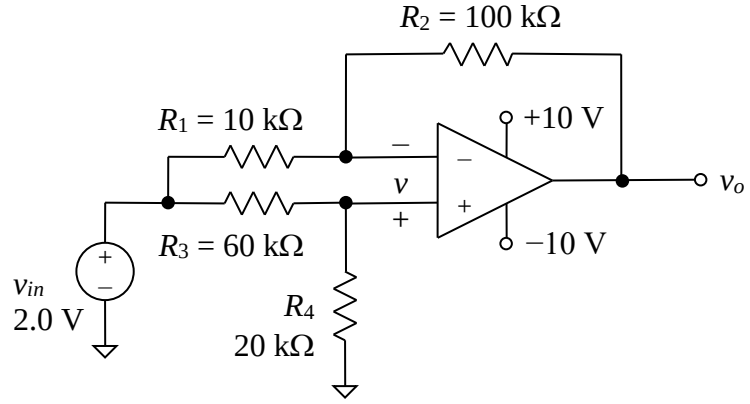
Note that the first few problems will be graded and the rest will not be graded. Only the graded problems must be submitted by the deadline above; do not submit the ungraded problems.

***Graded Problems:***

**1.** The input signal $v_{in}$ supplied to the amplifier circuit shown below is an AC voltage that can be expressed as $v_{in}(t) = V_m \cos(32{,}000\pi t - 60°)$ V, where $V_m$ is the amplitude of the voltage. Find the maximum value that $V_m$ can have to avoid clipping of the output voltage $v_o$. Assume that the actual output voltage limits are +8.5 V and −8.0 V. You may ignore the effects of the input offset voltage and input bias currents since they will be negligible in this case.




**2.** Show that the op-amp in the circuit diagram below saturates at one of the power supply voltages, and find the resulting voltages $v$ and $v_o$. Note that the circuit is not a diff amp because $R_4/R_3 \neq R_2/R_1$, not even approximately. You may ignore the minor effects of the input offset voltage and input bias currents of the op-amp. Assume that $v_o$ can swing all the way from −10 V to +10 V.

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3. **[deferred from HW #2]** Suppose that you have been asked to design a new digital data link, and the system needs a basic diff amp like the one shown in Figure 2.16 in the textbook (Sedra & Smith, 8th ed.). The differential-mode gain must be around 20 V/V, and the differential-mode input resistance must be $R_{id}$ = 50 kΩ. The power supply voltages are to be ±10 V. The selected op-amp has a maximum rated output current of 30 mA, a maximum input bias current of 20 nA, and a peak input offset voltage magnitude of 1.5 mV. Find the maximum allowable tolerance for the resistors $R_1$ through $R_4$ to ensure that the CMRR of the diff amp would be at least 75 dB.

4. In the supplemental reading "Real-World Performance of Difference Amplifiers," it is shown that the worst-case CMRR for a diff amp occurs when

$$R_1 = (1-\varepsilon)R_{1nom} \qquad R_2 = (1+\varepsilon)R_{2nom} \qquad R_3 = (1+\varepsilon)R_{3nom} \qquad R_4 = (1-\varepsilon)R_{4nom},$$

where the "nom" subscript indicates the nominal (ideal) value of the resistor and where $\varepsilon$ is the fractional tolerance (e.g., $\varepsilon$ = 0.05 corresponds to 5%). Alternatively, if the "+" signs are replaced with "–" signs and vice versa, the same result is obtained. Using the worst-case resistor values given above, show that the approximation given below left is valid regardless of the resistor values. In a diff amp, the nominal resistor values have the relationship given below right.

$$1-\frac{R_2}{R_1}\frac{R_3}{R_4} \approx 4\varepsilon \qquad\qquad \frac{R_{2nom}}{R_{1nom}}\frac{R_{3nom}}{R_{4nom}} = 1$$

5. **[deferred to HW #4]** The diff amp circuit shown on the next page is meant to scale up the differential voltage produced by a pair of strain gauges arranged in a Wheatstone bridge. The strain gauge resistance $R_s$ has a nominal value of 300 Ω at the neutral position. The gauge factor is 2.0, which means that the fractional resistance change $\Delta R/R_{nom}$ from nominal is twice that of the strain (e.g., 0.1% strain yields $\Delta R/R_{nom}$ = 0.002). The two strain gauges are arranged so that when one gauge's resistance increases in value, the other's resistance decreases. The other two resistors (labeled $R_{fix}$) are fixed and have the indicated values to a very high precision. At a strain of 0.5%, the differential voltage $v_2 - v_1$ would be equal to 60 mV if an infinite resistance were connected across the bridge (i.e., between the nodes *A* and *B*). The diff amp is designed to amplify the bridge voltage by a factor of 40. Thus, for a bridge voltage of 60 mV, the diff amp output voltage should be 2.4 V. Find the actual differential-mode output voltage at a strain of 0.5% for the circuit shown below, and compare it to the ideal value of 2.4 V. The power supply voltages for the op-amp are ±12 V (not shown for clarity). *Hint*: Replace the Wheatstone circuit with a floating Thévenin equivalent circuit connected between nodes *A* and *B*.

6. **[deferred to HW #4]** Suppose that the resistors in the diff amp and Wheatstone bridge in the previous problem have values that are exactly as labeled. For a strain of 0.5%, the strain gauge on the left would have a value of 303 Ω, and the one on the right would have a value of 297 Ω. Because the strain gauge resistances are not equal, a common-mode voltage would appear at the output of the op-amp. Find its value.

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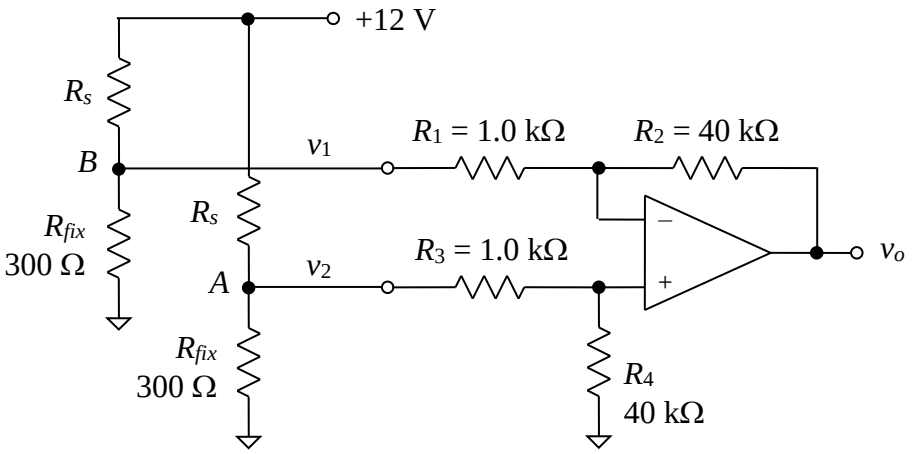
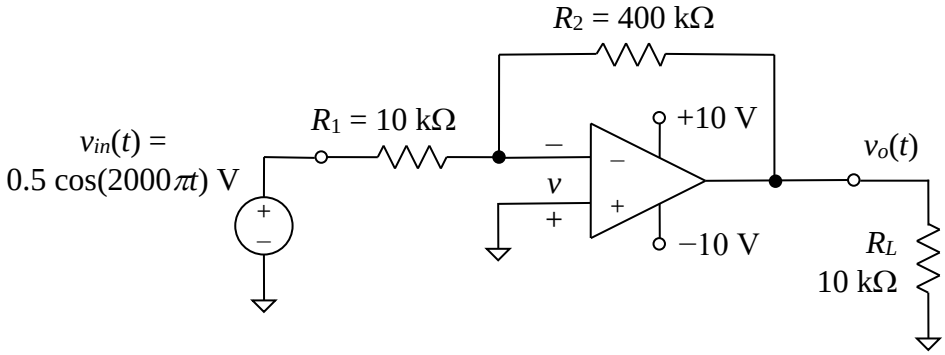



**Circuit diagram for Graded Probs. 5 and 6**

***Ungraded Problems*:**

The following problems will not be graded. They are intended to serve as practice problems and examples. You should attempt to solve them on your own and then check the solutions afterwards. Do not give up too quickly if you struggle to solve any of them. Move on to a different problem and then come back to the difficult one after a few hours.

**1.** Sketch at least one cycle of the voltage $v$ as a function of time for the circuit shown below. The amplifier goes into saturation (i.e., the output clips) during parts of the AC cycle. Find the first four instances in time after $t = 0$ when the amplifiers transitions from linear operation to clipping or vice versa. The load is another amplifier with an input resistance represented by the equivalent resistance $R_L$. (That is, the load resistance of the amplifier below is the same as the input resistance of the following amplifier.) You may ignore the input offset voltage and input bias currents of the op-amp.




**2.** For the amplifier circuit considered in the previous problem, assume that the magnitude of the input voltage $v_{in}$ is reduced from 0.5 V to 0.1 V and the load is replaced with a new one with an equivalent resistance $R_L$ of 100 Ω. If the output current limit rating of the op-amp is 25 mA, sketch the output waveform for one complete AC cycle. You may ignore the input offset voltage and input bias currents of the op-amp.

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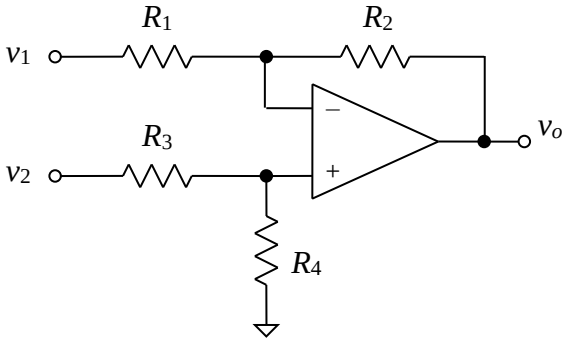
**3.** For the circuit considered in the previous two problems, find the voltage $v$ at the instant when the input voltage $v_{in}$ is at its peak positive value.

**4.** For the basic diff amp circuit depicted below, use a derivation like the one outlined in the supplemental notes "Real-World Performance of Difference Amplifiers" to show that a good approximation of the worst-case common-mode gain is given by the expression for $A_{cm}$ given below. You may assume that the resistor value ratios satisfy the given approximation.




$$A_{cm} \approx 4\varepsilon \frac{R_2}{R_1 + R_2}$$

$$\frac{R_4}{R_3} \approx \frac{R_2}{R_1}$$