ECEG 350 Electronics I Fall 2023

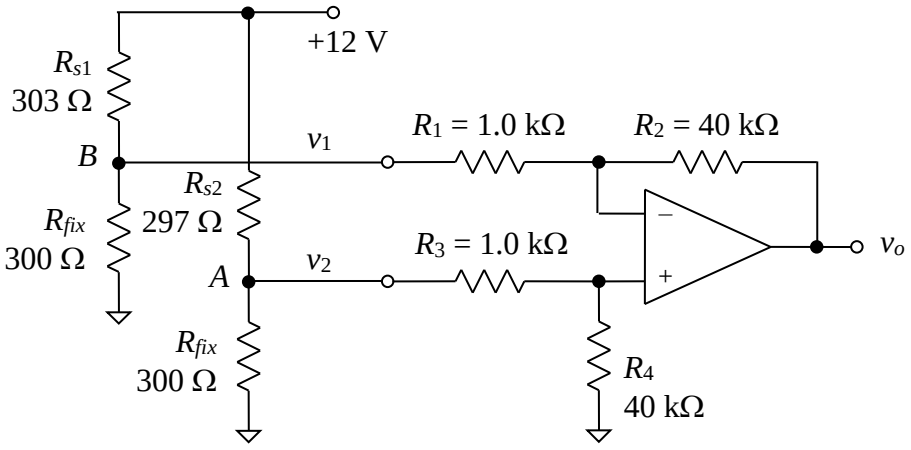
Homework Assignment #4 – due via Moodle at 11:59 pm on Friday, Sept. 22, 2023

***Instructions, notes, and hints*:**

You may make reasonable assumptions and approximations in order to compensate for missing information, if any. Provide the details of all solutions, including important intermediate steps. You will not receive credit if you do not show your work.

***Graded Problems*:**

1. **[deferred from HW #3 and modified]** The diff amp circuit shown below is meant to scale up the differential voltage produced by a pair of strain gauges arranged in a Wheatstone bridge. The strain gauge resistances R_{s1} and R_{s2} each has a nominal value of 300 Ω at the neutral position. The gauge factor is 2.0, which means that the fractional resistance change $\Delta R/R_{nom}$ from nominal is twice that of the strain (e.g., 0.1% strain yields $\Delta R/R_{nom} = 0.002$). The two strain gauges are arranged so that when one gauge's resistance increases in value, the other's resistance decreases. The other two resistors (labeled R_{fix}) are fixed and have the indicated values to a very high precision. At a strain of 0.5%, the differential voltage $v_2 - v_1$ would be equal to 60 mV if an infinite resistance were connected across the bridge (i.e., between the nodes *A* and *B*). The diff amp is designed to amplify the bridge voltage by a factor of 40. Thus, for a bridge voltage of 60 mV, the diff amp output voltage should be 2.4 V. Using the differential input resistance of the diff amp, estimate the output voltage actually obtained at a strain of 0.5%, and compare it to the ideal value of 2.4 V. The power supply voltages for the op-amp are ±12 V (not shown for clarity). *Hint*: Replace the Wheatstone circuit with a floating Thévenin equivalent circuit connected between nodes *A* and *B*.



2. **[deferred from HW #3 and modified]** Suppose that the resistors in the diff amp and Wheatstone bridge in the previous problem have values that are exactly as labeled. Use the superposition principle to find the actual output voltage. That is, find the output voltage due to the +12 V source, R_{fix}, and R_{s1} connected to node B and the output voltage due to the +12 V source, R_{fix}, and R_{s2} connected to node A, and then add them together. The value found in this problem the one from the previous problem do not exactly match, but they are close.

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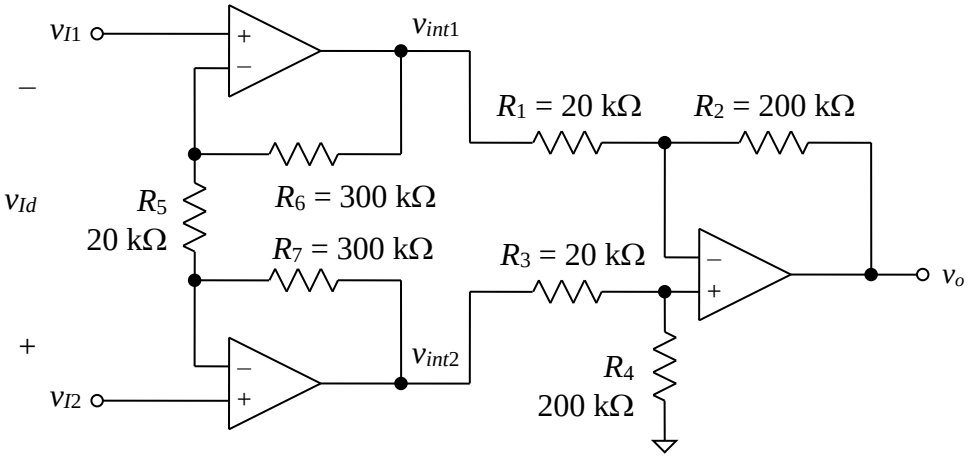
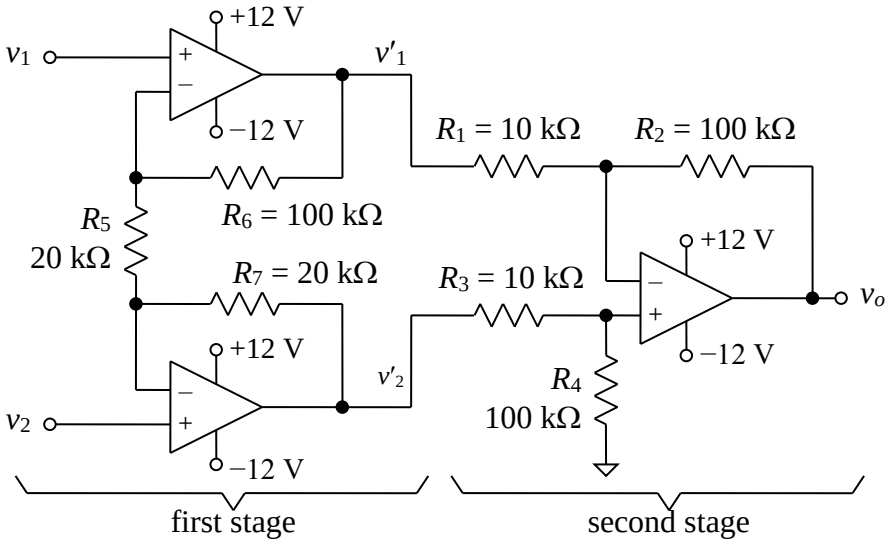
3. The resistors in the instrumentation amplifier shown below are labeled with their nominal values. A sinusoidal differential-mode voltage with the waveform given by the expression below is applied across the input terminals of the amplifier (between nodes v_{I1} and v_{I2}). The common-mode voltage gain of the second stage is 0.028 V/V. Find the resulting peak-to-peak differential voltage $v_{int2} - v_{int1}$ and peak-to-peak differential output voltage v_{od}. The power supply voltages are ±15 V but are not shown in the diagram to improve clarity.

$$v_{Id}(t) = 0.44\cos(2,200\pi t - 50°) \text{ mV}$$



4. Suppose that nearby building wiring causes a common-mode periodic signal with a peak-to-peak voltage of 120 mVpp and a frequency of 60 Hz to appear at the two inputs of the instrumentation amplifier considered in the previous problem. All of the resistor values are the same as in the previous problem as is the common-mode gain of the second stage. Ignoring the differential-mode input voltage, find the peak-to-peak common-mode node voltages at the v_{int1}, v_{int2}, and v_o nodes.

5. The instrumentation amplifier shown below was accidentally assembled with the wrong value for resistor R_7; its value should have been 100 kΩ. All resistors have 5% tolerance; the values shown are the nominal ones. If the common-mode gain A_{cm2} of the second stage is 0.0044 V/V, find the differential-mode and common-mode gains of the full amplifier to reasonably good approximations (accurate to ±5% or so).



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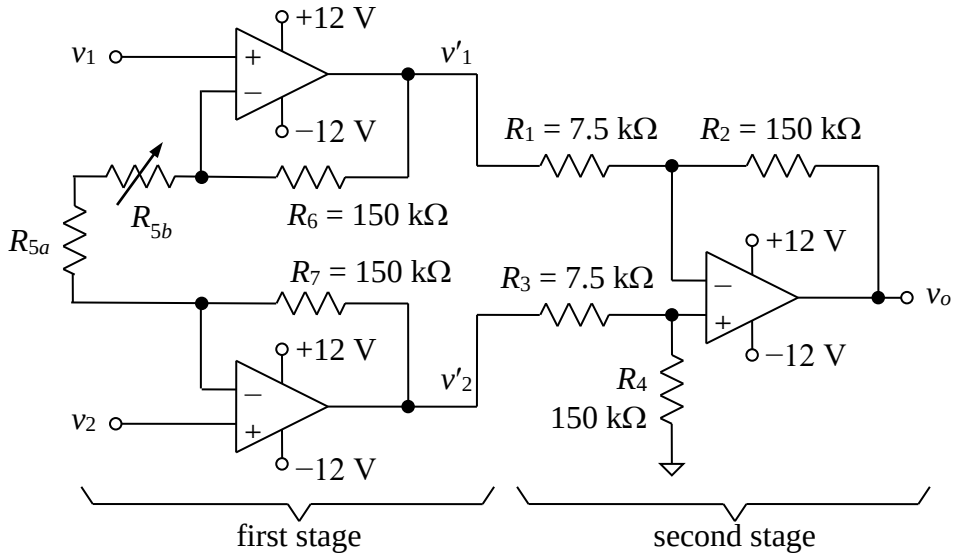
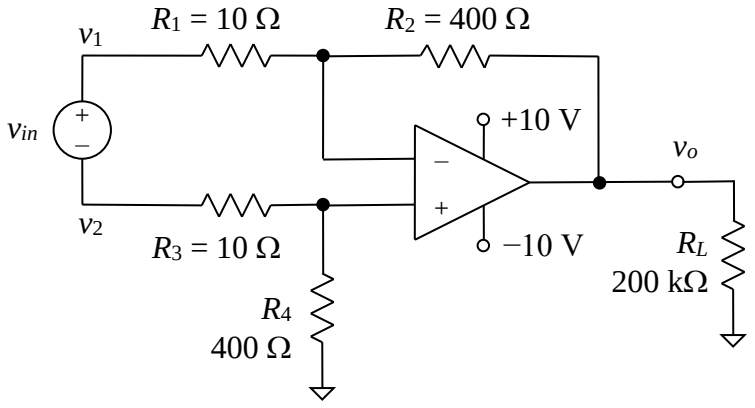
6. The instrumentation amplifier depicted below uses 1% tolerance resistors in the first stage and 0.1% tolerance resistors in the second stage. The circuit is unusual in that resistor R_5 has been split into a fixed portion R_{5a} and a variable portion R_{5b}. The variable resistor can have a minimum value of zero and a maximum value $R_{5b\max}$. Find the required values for R_{5a} and $R_{5b\max}$ so that the overall nominal differential-mode gain varies from 40 to 100 V/V. Also find the lowest possible overall CMRR value (expressed in dB) obtained as R_{5b} is varied over its full range of values. That is, find the worst-case CMRR obtained over the full range of differential-mode gains from A_d = 40 to 100 V/V.



***Ungraded Problems*:**

The following problems will not be graded. They are intended to serve as practice problems and examples. The solutions to these problems will be posted along with those to the graded ones.

1. The op-amp in the diff amplifier shown below has an output current magnitude limit of 10 mA. The resistor values used in the circuit are ridiculously small; this problem helps to illustrate why. Input voltage v_{in} can be as high as ±250 mV before the output saturates at one of the power supply limits (±10 V here). However, output current limiting prevents the output voltage from reaching that level. If v_{in} = −250 mV (DC), find the resulting voltage v across the input terminals of the op-amp (positive side of v at the "+" terminal). *Hint*: Check whether the load connected to the output of the circuit has a high enough equivalent resistance so that the current flowing through it can be considered negligible.



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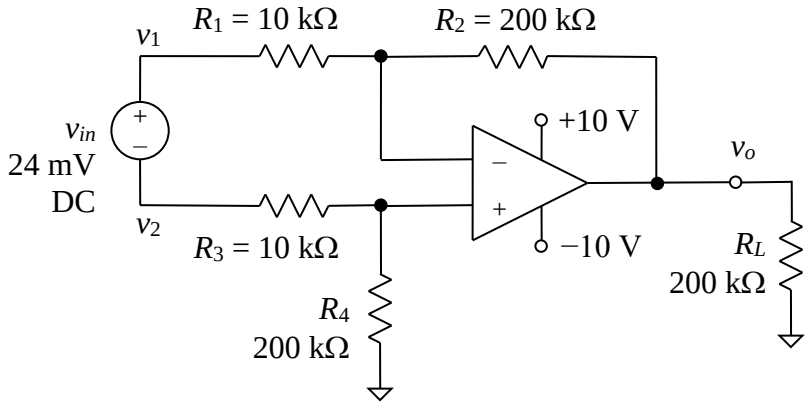
2. The resistors in the diff amp circuit diagram below are labeled with their nominal (ideal) values. Each one has a 2% tolerance. The actual resistor values (to four-digit accuracy) are R_1 = 10.10 kΩ, R_2 = 196.4 kΩ, R_3 = 10.14 kΩ, and R_4 =198.8 kΩ. The input voltage is quasi-DC (i.e., very slowly varying) and currently has a value of 24 mV. Although not shown in the diagram, the sensor generating the input voltage is connected to the amplifier using a very long cable in a noisy environment. The strongest noise source is the building's AC wiring, and it causes a common-mode input voltage expressed as $v_{Icm}(t) = 0.140 \cos(377t)$ V to appear at each input of the amplifier. Note that $|v_{in}| < |v_{Icm}|_{pk}$. Find:

a. the nominal differential-mode gain (i.e., the gain assuming ideal resistor values).
b. the actual differential-mode gain A_d (using actual resistor values).
c. the actual common-mode gain A_{cm}.
d. the actual CMRR (in dB).
e. the differential-mode output voltage v_{od}.
f. the common-mode output voltage v_{ocm}.



3. Suppose that the resistors in the diff amp in the previous problem are replaced with units having 5% tolerance. The actual resistor values are now R_1 = 10.42 kΩ, R_2 = 191.0 kΩ, R_3 = 10.38 kΩ, and R_4 = 205.6 kΩ. Repeat parts a through f of the previous problem. Comment on the relative changes of the differential-mode gain and the common-mode gain.

4. In the circuit shown on the next page, the op-amp is not ideal and has input bias currents of roughly 80 nA flowing into each terminal (i.e., $I_{B1} \approx I_{B2}$). Find the approximate output voltage v_o (to two digits of accuracy since the resistor values are given to only two digits) due only to the two input bias currents (i.e., for the case $v_1 = v_2 = V_{OS} = 0$) for the following two sets of values for resistors R_3 and R_4, and explain the significance of the results. The resistor tolerances are 0.1%. Note that the differential-mode gain is the same (15 V/V) for both parts.

a. R_3 = 200 kΩ and R_4 = 3.0 MΩ (same as R_1 and R_2)
b. R_3 = 10 kΩ and R_4 = 150 kΩ (same ratio as R_2/R_1)

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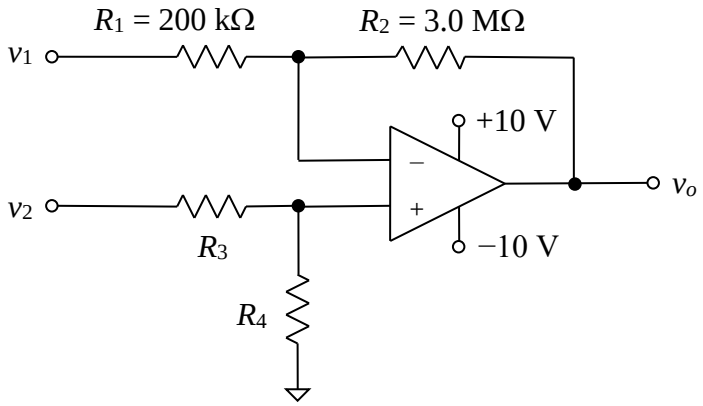
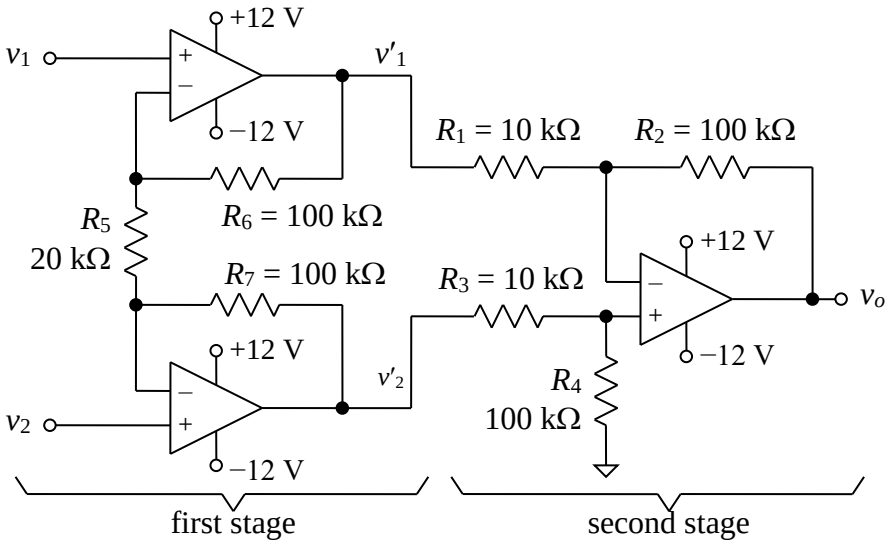


Circuit diagram for Ungraded Prob. 4

5. The instrumentation amplifier shown below is to be assembled using 5% tolerance resistors in the first stage, but the second stage will incorporate resistors manufactured using a precision laser cutting method. The resistor values shown are the nominal values. Find the resistor tolerance in the second stage required to guarantee that the CMRR will be at least 120 dB.



6. Now suppose that resistor R_5 in the previous problem is split into two resistors of equal value (i.e., each is 10 kΩ) and a connection to ground is added to the node between them. The new circuit would have the form shown on the next page. Find the constraint on the resistor tolerances in the second stage that would be necessary to again achieve a CMRR of at least 120 dB. The first-stage resistors would still have 5% tolerances. Compare this answer to the one for the previous problem.

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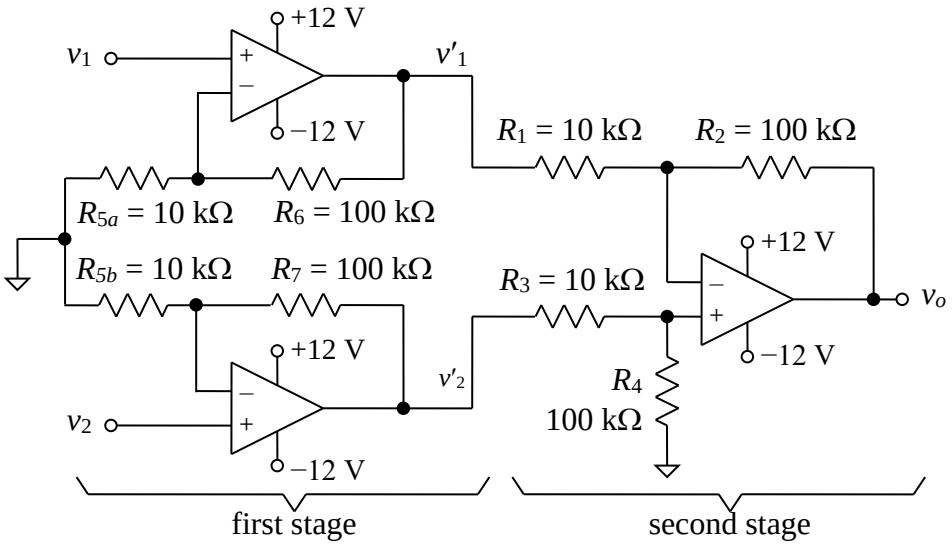

Circuit diagram for Ungraded Prob. 6

7. As in one of the graded problems, the amplifier shown below was assembled with the wrong value for resistor R_7. Note that the diagram does not depict a true instrumentation amplifier because resistor R_5 has been split into two 10 kΩ resistors and a connection to ground has been added between them. The common-mode gain A_{cm2} of the second stage is still 0.0044 V/V. Find reasonably good approximations of the differential-mode and common-mode gains of the full amplifier. This problem is somewhat challenging. You need to understand clearly how the differential-mode and common-mode gains are defined. You also need to be careful how you calculate the output voltage for the two types of input signals.