ECEG 350 Electronics I Fall 2025

Homework Assignment #5 – due via Moodle at 11:59 pm on Monday, Nov. 3, 2025

***Instructions, notes, and hints*:**

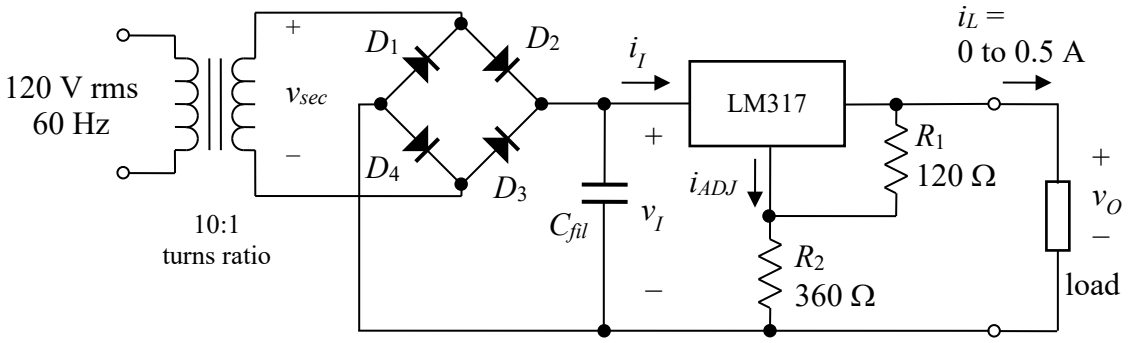
You may make reasonable assumptions and approximations to compensate for missing information, if any. Provide the details of all solutions, including important intermediate steps. You will not receive credit if you do not show your work.

The first few problems will be graded and the rest will not be graded. Only the graded problems must be submitted by the deadline above. Do not submit the ungraded problems.

***Graded Problems*:**

1. As shown below, an LM317 voltage regulator is used in a power supply circuit that includes a full-wave bridge rectifier and a filter capacitor C_{fil}. The rectifier diodes each have a turn-on voltage of V_F = 1.0 V, and the transformer's specified secondary winding voltage is 12 Vrms. The values of resistors R_1 and R_2 have been set to produce a nominal output (load) voltage of v_O = 5.0 V. The largest expected load current is 500 mA. The drop-out voltage V_{DO} of the regulator is about 2 V. A datasheet for the LM117 and LM317 is available on the Laboratory page at the ECEG 350 course web site.

- **a.** By KCL, if the current i_{ADJ} in the common terminal of the regulator is negligible, then the input current i_I to the regulator circuit must be approximately the same as the load current i_L for large values of load current. About 10 mA flows through R_1 and R_2 at all times. Find the required value of capacitor C_{fil} so that the minimum voltage $V_{\min}$ across the capacitor is roughly 80% greater than $v_O + V_{DO}$.
- **b.** Find the worst-case ripple on the capacitor voltage for the case when the load draws a DC output current at the maximum value of 0.5 A. Assume that C_{fil} has the value found in part a.
- **c.** Find the approximate time-average power dissipation of the LM317 at full output current (i_L = 500 mA).
- **d.** Use the information given in the datasheet to express the load regulation in mV/mA. Assume a typical case at 25 °C for the TO-220 package. Note that the data are given for an output current ranging from 10 mA to I_{MAX} = 1.5 A.



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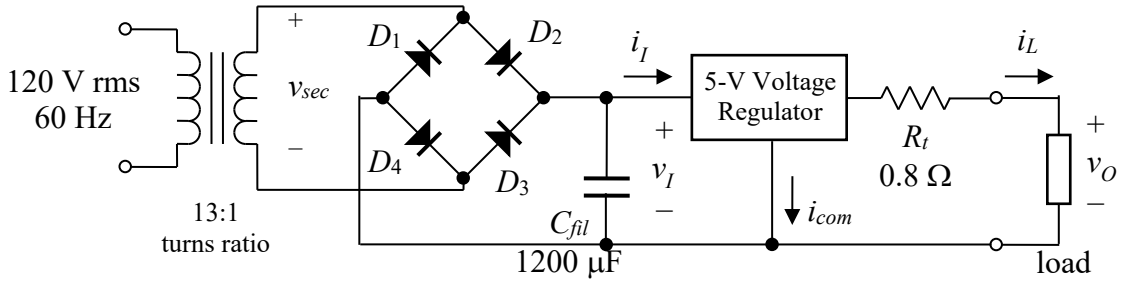
2. In the power supply circuit shown below, a three-terminal regulator provides a nominal voltage of 5 V to an amplifier module. Because of poor design technique, the circuit board trace between the output terminal of the regulator and the positive power supply terminal (the circle near the positive side of v_O) is too thin and has an equivalent resistance of 0.8 Ω. It is modeled as R_t in the diagram. The regulator itself has a specified load regulation of 0.008 mV/mA. Find the load regulation of the power supply circuit as a whole (i.e., including the effect of R_t). The rectifier diodes each have a turn-on voltage of 1.0 V, and the power supply is designed to provide up to 500 mA of current to the load. The current i_{com} (like i_{ADJ} in an adjustable regulator) is negligibly small.



3. For the power supply circuit considered in the previous problem, find:

- **a.** the approximate ripple voltage across the filter capacitor C_{fil} at the maximum load current (500 mA).
- **b.** the approximate time-average power dissipated by the three-terminal regulator.
- **c.** the line regulation expressed in the %/V unit, assuming that measurements reveal an output voltage ripple of 10 mV at the maximum load current of 500 mA.

4. Convert the line regulation specification 0.05%/V to the mV/V unit for the case when the nominal output voltage of a regulator is 12 V and the maximum load current is 500 mA.

5. The datasheet for the LM7805 fixed voltage regulator specifies the typical load regulation under the two different conditions listed below. The value given is the change in voltage over the specified change in output current. For each condition, express the load regulation in the mV/mA unit. Speculate on why two different results are obtained.

- **a.** Load regulation is 9.0 mV for output current variation from 5 mA to 1.5 A
- **b.** Load regulation is 4.0 mV for output current variation from 250 mA to 750 mA.

6. The NMOS device in the circuit shown on the next page has the parameter values k_n = 1.0 mA/V^2, V_t = 1.0 V, and $\lambda = 0$. (Parameter λ is related to the channel length modulation effect. If $\lambda = 0$, then the drain current is constant in the saturation region for any v_{DS} value.)

- **a.** Determine the region of operation of the MOSFET, and find the values of the drain-to-source voltage v_{DS} and drain current i_D. *Hint*: The solution of a quadratic equation might be necessary.
- **b.** Suppose that the drain resistor R_D is changed to 500 Ω. Determine (and confirm) the region of operation, and find the new values of i_D and v_{DS}.

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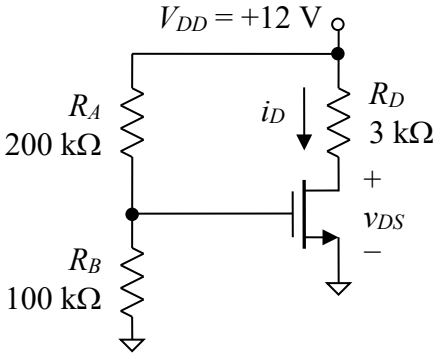


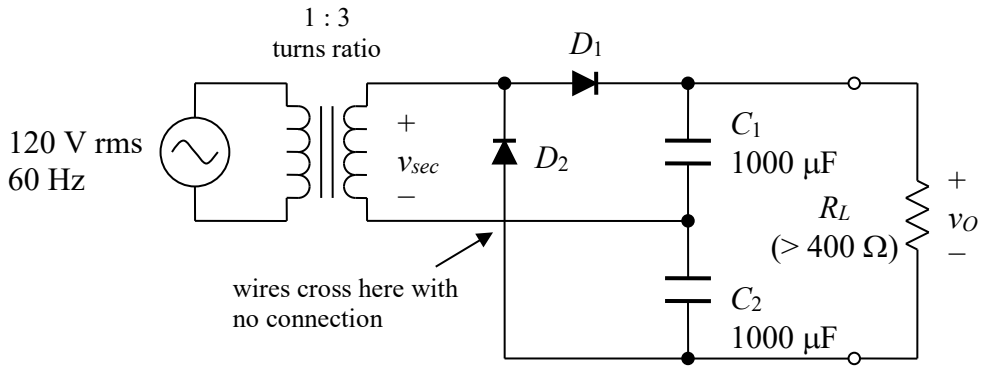
Circuit diagram for Graded Prob. 6

***Ungraded Problems*:**

The following problems will not be graded, but you should attempt to solve them on your own and then check the solutions. Do not give up too quickly if you struggle with one or more of them. Move on to a different problem and then come back to the difficult one after a few hours.

1. The power supply circuit shown below is typical of those used to drive high-voltage circuits. Note that it uses a step-up transformer. Also note that the output voltage v_O is the sum of the two capacitor voltages. The load has a minimum equivalent resistance of 400 Ω, but it could be higher. ($R_{L\text{min}}$ is associated with the maximum possible load current. Smaller load currents correspond to larger equivalent load resistances.) Complete the following analysis steps:

- **a.** Find the peak value of the secondary voltage v_{sec} of the transformer.
- **b.** Find the peak voltages across capacitors C_1 and C_2 if D_1 and D_2 are silicon diodes with turn-on voltages that are negligible compared to the secondary voltage.
- **c.** Find the approximate nominal output voltage v_O if the ripple voltage is negligibly small. *Hint*: This circuit called a *voltage doubler*, but you must show/explain why.
- **d.** Find the worst-case ripple voltage at the output (across the load R_L). The diodes conduct for only a tiny fraction of each period of the secondary voltage.
- **e.** Find the peak reverse-bias voltage experienced by each diode, assuming in this case that the voltages across C_1 and C_2 have negligible ripple.



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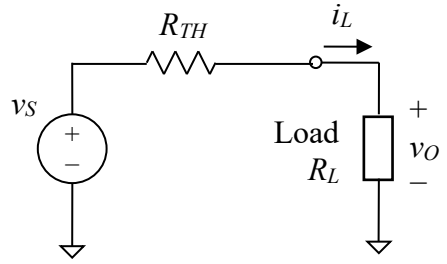
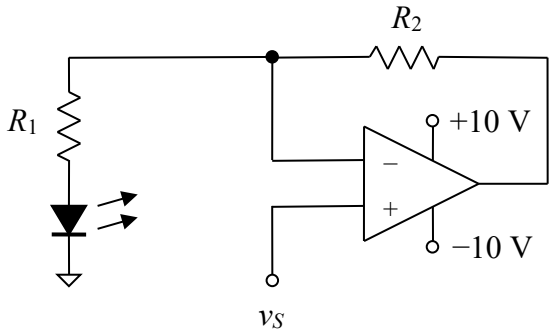
2. Show that the expression for dv_O/di_L for any TEC like the one shown below right is equal to the negative of the Thévenin equivalent resistance; that is, prove the expression shown below left. Note that dv_O/di_L is equal to the load regulation for a voltage regulator circuit if the minus sign is ignored. Also note that $dv_O/di_L = \Delta v_O/\Delta i_L$ for the case of a purely resistive (real-valued) load and a purely resistive Thévenin equivalent impedance.

$$\frac{dv_O}{di_L} = -R_{TH}$$



3. The circuit shown below is designed to light the LED when voltage v_S ("S" subscript for "sense") is above the turn-on voltage of the LED, which is $V_F = 1.8$ V. The LED shines brighter as v_S rises. However, above a certain value of v_S the LED stops increasing in brightness as v_S continues to rise. Assuming that the constant-voltage model applies for the LED, find the standard 5% values of R_1 and R_2 that would cause the LED to reaches its maximum brightness at around $v_S = 5.0$ V and so that the maximum current through the LED is around 25 mA. The op-amp has the specifications given next to the figure. *Hint*: Aspects of the problem that do not have a significant impact on the determination of the resistor values can be ignored.



<u>Op-Amp:</u>
max. input offset voltage magnitude: 8.0 mV
max. input bias current: 100 nA
typ. open-loop voltage gain: 1.5×10^5
output voltage limits: ±9.0 V
output current limit: 35 mA