ECEG 350 **Electronics I** **Fall 2023**

Homework Assignment #7 – due via Moodle at 11:59 pm on Friday, Nov. 3, 2023

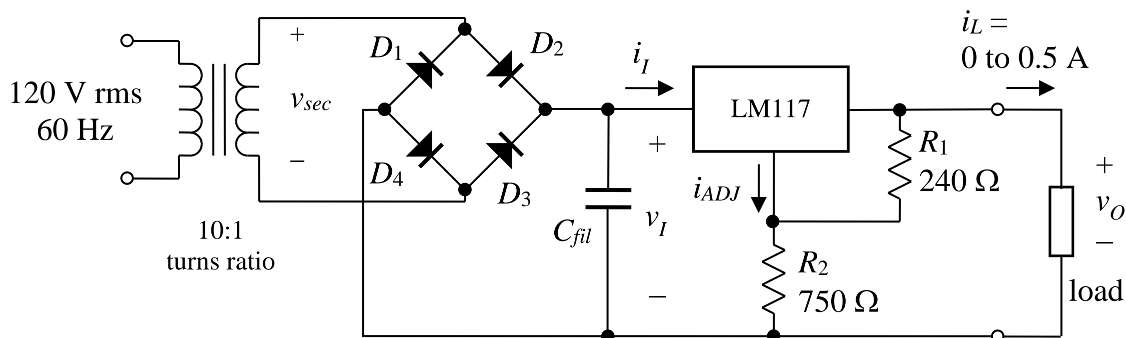
***Instructions, notes, and hints*:**

You may make reasonable assumptions and approximations in order to compensate for missing information, if any. Provide the details of all solutions, including important intermediate steps. You will not receive credit if you do not show your work.

***Graded Problems*:**

1. **[deferred from HW #6]** As shown below, an LM117 voltage regulator is used in a power supply circuit that includes a full-wave bridge rectifier and a filter capacitor C_{fil}. The rectifier diodes each have a turn-on voltage of $V_F = 1.0$ V, and the transformer's specified secondary winding voltage is 12 V rms. The values of resistors R_1 and R_2 have been set to produce a nominal output (load) voltage of $v_O = 5.2$ V. The largest expected load current is 500 mA. The drop-out voltage V_{DO} of the regulator is about 2 V.

   Use the information given in the LM117/LM317 datasheet (available on the Laboratory page at the ECEG 350 course web site) to express the load regulation in mV/mA. Assume a typical case at 25 °C for the TO-220 package. Note that the data are given for an output current range of 10 mA to $I_{\text{MAX}} = 1.5$ A.



2. **[deferred from HW #6]** In the power supply circuit shown on the next page, a three-terminal regulator provides a nominal voltage of 5 V to a load. Because of poor design technique, the circuit board trace between the output terminal of the regulator and the positive power supply terminal (the circle near the positive side of v_O) is too thin and has an equivalent resistance of 0.8 Ω. It is modeled as R_t in the diagram. The regulator itself has a specified load regulation of 0.008 mV/mA. Find the load regulation of the power supply circuit, including the effect of R_t. The rectifier diodes each have a turn-on voltage of 1.0 V, and the power supply is designed to provide up to 500 mA of current to the load. The current i_{com} is negligibly small.

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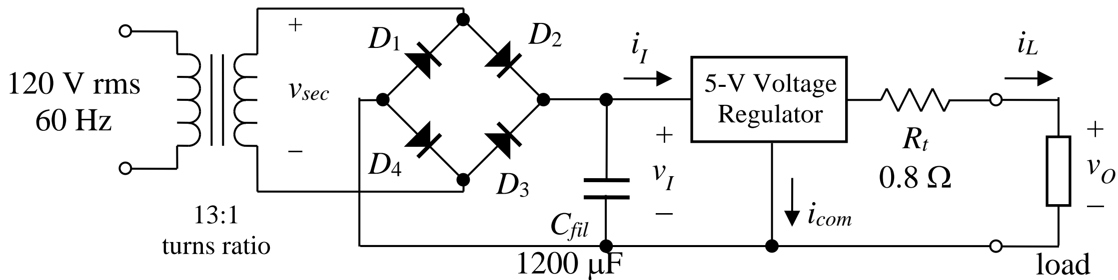


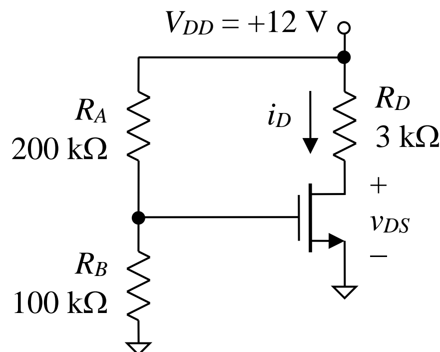
Circuit diagram for Graded Problem 2.

3. **[deferred from HW #6]** For the power supply circuit considered in the previous problem, find the line regulation expressed in the %/V unit assuming that measurements reveal an output voltage ripple of 10 mV at the maximum load current of 500 mA.

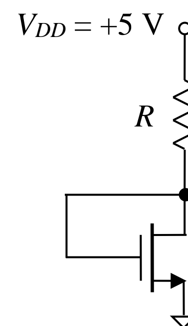
4. The NMOS device in the circuit shown below has the parameter values $k_n = 1.0$ mA/V^2, $V_t = 1.0$ V, and $\lambda = 0$. (Parameter λ is related to the channel length modulation effect. If $\lambda = 0$, then the drain current is constant in the saturation region for all values of v_{DS}.)

   a. Determine the region of operation of the MOSFET, and find the values of the drain-to-source voltage v_{DS} and drain current i_D. *Hint*: The solution of a quadratic equation might be necessary.

   b. Suppose that the drain resistor R_D is changed to 500 Ω. Determine (and confirm) the region of operation, and find the new values of i_D and v_{DS}.



5. The "diode-connected" NMOS device in the circuit shown to the right is fabricated using the 0.8 μm process. The approximate parameter values are $V_t = 0.7$ V, $L = 0.8$ μm (channel length), and $\mu_n C_{ox} = 130$ μA/V^2. Find the required values for the channel width W and the resistance R to establish a drain-to-source voltage V_{DS} of 2.5 V and a drain current i_D of 3.0 mA. You may ignore the channel-length modulation effect (i.e., assume that $\lambda = 0$).



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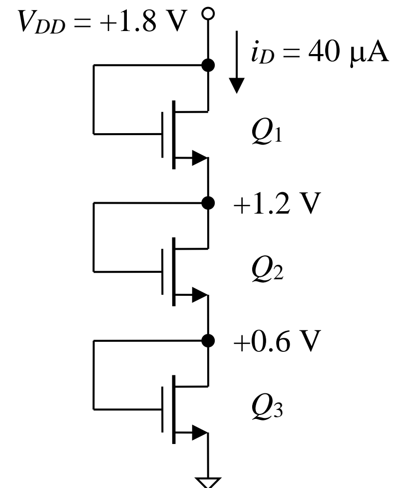
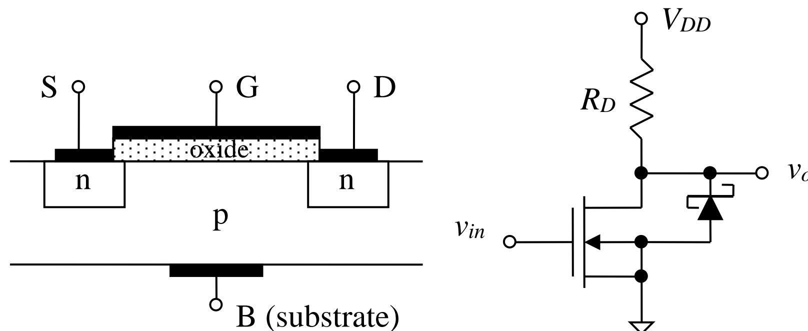
6. The MOSFETs in the circuit shown to the right are fabricated using the 0.18 μm process on the same silicon substrate and all have $V_t = 0.50$ V, $\mu_n C_{ox} = 390$ μA/V^2, and $L = 0.18$ μm. Assuming that $\lambda = 0$ (i.e., neglect the channel-length modulation effect), find the required MOSFET gate widths (W_1, W_2, and W_3) to obtain the indicated node voltages and drain current. MOSFET "stacks" like these are sometimes used to establish bias and reference voltages in integrated circuits. A MOSFET that has its gate connected to its drain, like the ones shown to the right, is sometimes referred to as "diode-connected." This is a carryover from BJT terminology where a similar BJT configuration (base connected to collector) acts like a *pn* junction diode.



***Ungraded Problems*:**

The following problems will not be graded, but you should attempt to solve them on your own and then check the solutions. Do not give up too quickly if you struggle with one or more of them. Move on to a different problem and then come back to the difficult one after a few hours.

1. The diagram below left depicts the internal structure of an *n*-channel enhancement-mode MOSFET. In the diagram to the right, the same MOSFET is used in a basic inverter circuit. Also indicated in the circuit diagram is a Schottky diode that has been added between the substrate terminal and the drain terminal. MOSFET manufacturers often add Schottky diodes like this and in other locations as protective measures, especially in CMOS circuits. Give a valid explanation for the presence of the diode in the circuit. An important point (and hint) is that Schottky diodes have lower turn-on voltages (approximately 0.3 V) than standard silicon *pn* junction diodes.



2. The n-channel MOSFET in the circuit on the next page has $k_n = 800$ μA/V^2 and $V_t = 0.70$ V and is operating with a bipolar (±3.3 V) power supply. Find the values of R_S and R_D that yield a drain current I_D of 1.0 mA and a value for V_{DS} that is 0.50 V above the triode-saturation boundary (defined by $V_{DS} = V_{GS} - V_t$). Assume that $\lambda = 0$ (i.e., there is no channel-length modulation). Note that the value of R_G theoretically does not have an impact on the DC current voltage levels in the circuit because the quiescent gate current is zero. In fact, R_G could be set to zero if the DC performance were the only concern. However, we will see that there are practical reasons why R_G should be set to a very large value.

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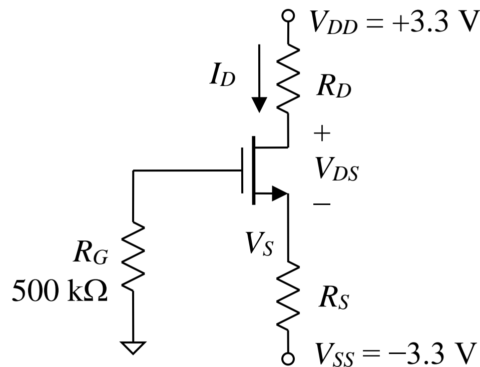

Circuit diagram for Ungraded Problem 2.

3. Measurements are performed on an *n*-channel MOSFET in a test configuration that has the gate shorted to the drain. It is found that the DC drain current is 0.40 mA for $V_{GS} = V_{DS} =$ 1 .0 VDC and 0.10 mA for $V_{GS} = V_{DS} = 0.80$ V. Use the measured data to estimate the values of k_n and V_t for the MOSFET. The tests assume that $\lambda = 0$ (i.e., there is no channel length modulation).

4. As explained in Sec. 5.4.4 of the textbook (Sedra & Smith, 8th ed.), the MOSFET parameter values k'_n and V_{tn} are sensitive to temperature. (Recall that $k_n = k'_n\, W/L$ and that $k'_n = \mu_n C_{ox}$.) Both values decrease with rising temperature, but the changes have opposite effects on the drain current. While the effects are present whether the MOSFET operates in the saturation region or the triode region, their impacts are perhaps more obvious for the saturation case since the expression for i_D is simpler:

$$i_D = \frac{1}{2} k_n \left(v_{GS} - V_{tn} \right)^2 .$$

For a given value of v_{GS}, decreasing V_{tn} causes i_D to rise, whereas decreasing k_n causes i_D to fall. Because the change in V_{tn} is only about 2 mV/°C, the change in k_n usually dominates, so i_D usually decreases with increasing temperature in MOSFET circuits. However, if the overvoltage ($v_{GS} - V_{tn}$) is relatively small, say, a volt or less, then the change in V_{tn} can dominate, which causes i_D to rise overall with rising temperature. One example of a crossover from V_{tn} dominance to k_n dominance can be seen in Fig. 5 of the Fairchild Semiconductor 2N7000 datasheet available at the ECEG 350 Laboratory web page.

For the circuit shown at the top of the next page, assume that the overvoltage is large enough that the temperature variation of V_{tn} can be ignored and that $V_t \approx 1.0$ V at all temperatures. Also assume that $\lambda = 0$. Suppose that $k_n = 1.0$ mA/V^2 initially but then the temperature decreases, which causes k_n to rise. Find the value of k_n at which the MOSFET makes the transition from the saturation region to the triode region. By the way, temperature sensitivity is one reason why the circuit below is never used in practice to bias a MOSFET. A resistor (usually labeled R_S in Sedra & Smith) added in series with the source terminal greatly stabilizes the drain current against temperature changes.

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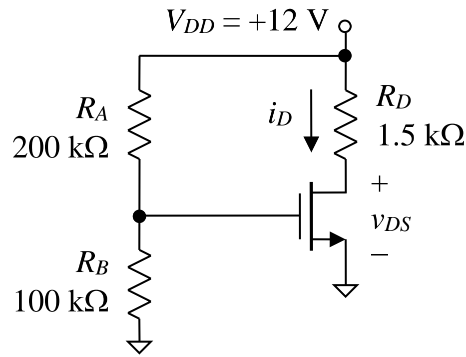

Circuit diagram for Ungraded Problem 4

5. Shown below is a four-resistor bias network that has already been designed. The MOSFET has the nominal parameter values $k_n = 4$ mA/V^2 and $V_t = 1.0$ V. Find the values of V_{GS} and V_{DS} under nominal conditions. How far (how many volts) above the saturation-triode boundary is V_{DS}? Note: The "$V_{DD}/3$" rule-of-thumb has *not* been applied to this circuit to determine the values of R_D and R_S. The rule-of-thumb is not used when other constraints apply.