ECEG 350 **Electronics I** **Fall 2026**

Homework Assignment #7 – due via Moodle at 11:59 pm on Monday, Nov. 9, 2026

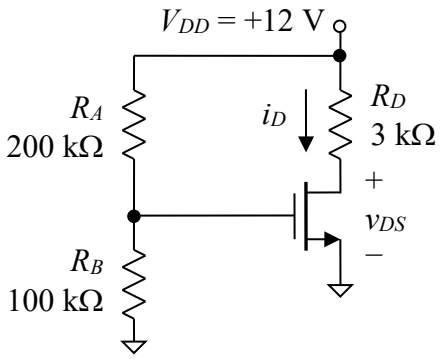
***Instructions, notes, and hints*:**

You may make reasonable assumptions and approximations to compensate for missing information, if any. Provide the details of all solutions, including important intermediate steps. You will not receive credit if you do not show your work.

The first few problems will be graded and the rest will not be graded. Only the graded problems must be submitted by the deadline above. Do not submit the ungraded problems.

***Graded Problems*:**

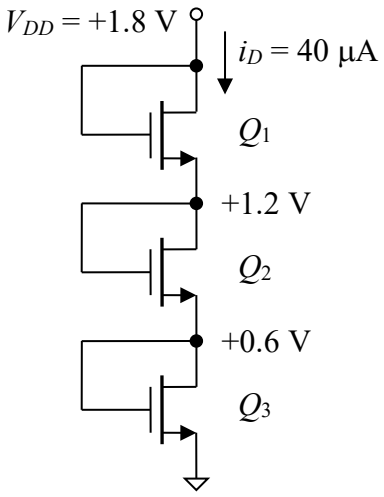
1. The NMOS device in the circuit shown to the right has the parameter values $k_n = 1.0$ mA/V^2, $V_t = 1.0$ V, and $\lambda = 0$. (Parameter λ is related to the channel length modulation effect. If $\lambda = 0$, then the drain current is constant in the saturation region for any v_{DS} value.)



   a. Determine the region of operation of the MOSFET, and find the values of the drain-to-source voltage v_{DS} and drain current i_D. *Hint*: The solution of a quadratic equation might be necessary.

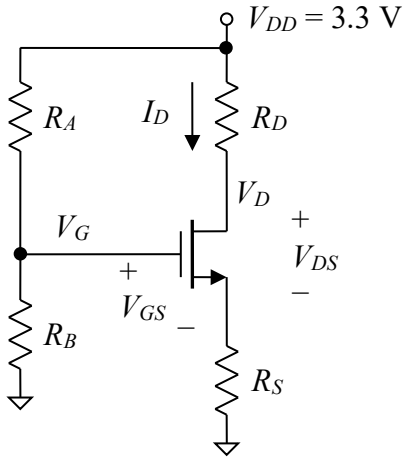
   b. Suppose that the drain resistor R_D is changed to 500 Ω. Determine (and confirm) the region of operation, and find the new values of i_D and v_{DS}.

2. The MOSFETs in the circuit shown to the right are fabricated using the 0.18 μm process on the same silicon substrate and all have $V_t = 0.50$ V, $\mu_n C_{ox} = 390$ μA/V^2, and $L = 0.18$ μm. Assuming that $\lambda = 0$ (i.e., the channel-length modulation effect can be neglected), find the required MOSFET gate widths (W_1, W_2, and W_3) to obtain the indicated node voltages and drain current. MOSFET "stacks" like these are sometimes used to establish bias and reference voltages in integrated circuits. A MOSFET that has its gate connected to its drain, like the ones shown to the right, is sometimes referred to as "diode-connected." This is a carryover from BJT terminology where a similar BJT configuration (base connected to collector) acts like a *pn* junction diode. *Hint*: It is impossible for a MOSFET to operate in one of the three regions of operation if it is diode-connected.



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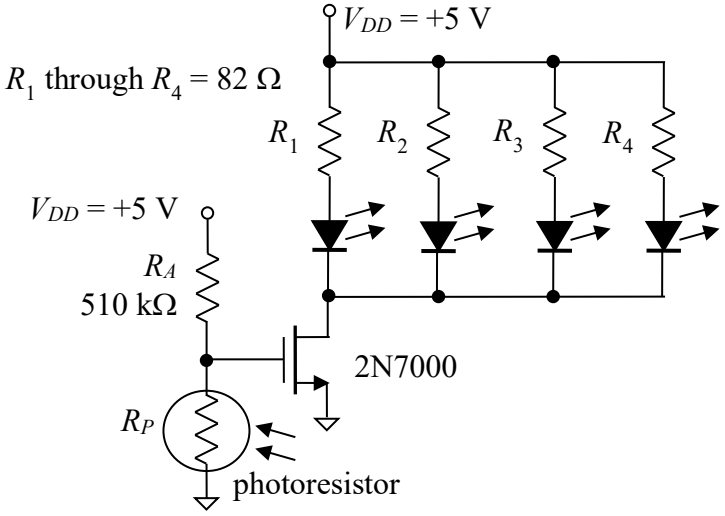
3. After a series of tests, it is found that the MOSFET in the circuit depicted below has a threshold voltage of $V_t = 0.8$ V and that the drain current is 500 μA when the device is operated in the saturation region with $v_{GS} = 1.2$ V. The measurement results help to determine the value of k_n. Assume that $\lambda = 0$ (i.e., no channel-length modulation).



a. Find the required resistor values so that $I_D = 300$ μA. Apply the standard rule-of-thumb that sets $I_D R_D = I_D R_S = V_{DS} = V_{DD}/3$, and choose the values of R_A and R_B so that $R_A \| R_B \geq 500$ kΩ. An infinite number of combinations of R_A and R_B values will work.

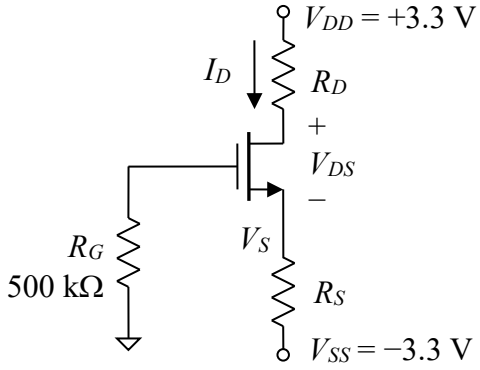
b. The designers discover that they need more "headroom" and "legroom" for the *total* node voltage v_D. (Headroom and legroom are the ranges of voltages over which v_D can vary above and below the quiescent voltage V_D to avoid operation in the cut-off and triode regions. The total range of v_D is sometimes called the "swing range.") The designers therefore decide to make $I_D R_S = 0.25 V_{DD}$ (the voltage across R_S) while keeping I_D the same. Find the required values of R_A, R_B, and R_S to allow for the change. Also find the value of R_D required to place quiescent node voltage V_D at the midpoint between $I_D R_S$ and V_{DD} (roughly equal headroom and legroom). The values of R_A and R_B should still be chosen so that $R_A \| R_B \geq 500$ kΩ.

4. As shown below, a 2N7000 MOSFET is used to switch four white LEDs on or off depending on the state of a photoresistor R_P. The resistance of R_P varies from around 300 Ω in bright conditions to around 3.0 MΩ in the dark. Assuming that all of the LEDs are identical and have turn-on voltages of 3.2 V, find the region of operation and the drain-to-source voltage of the 2N7000 when the light conditions are such that $R_P = 1.2$ MΩ. Also find the power dissipation of the MOSFET in this state. Assume that $V_t = 2.1$ V and $k_n = 200$ mA/V^2 for the 2N7000. The 2N7000 data sheet is available at the ECEG 350 Laboratory web page.

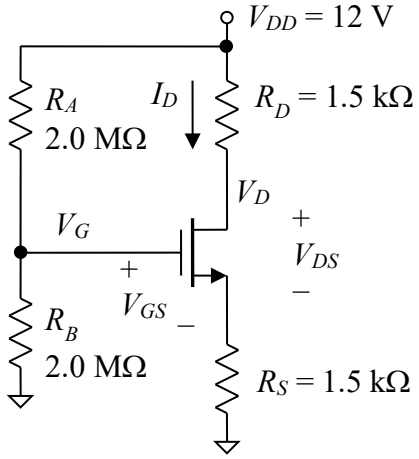


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5. The *n*-channel MOSFET in the circuit depicted to the right has $k_n = 800\ \mu A/V^2$ and $V_t = 0.70$ V and is operating with a bipolar (±3.3 V) power supply. Find the values of R_S and R_D that yield a drain current I_D of 1.0 mA and a value for V_{DS} that is 0.50 V above the triode-saturation boundary (defined by $V_{DS} = V_{GS} - V_t$). Assume that $\lambda = 0$ (i.e., there is no channel-length modulation). Note that the value of R_G theoretically does not have an impact on the DC current voltage levels in the circuit because the quiescent gate current is zero. In fact, R_G could be set to zero if the DC performance were the only concern. However, we will see that there are practical reasons why R_G should be set to a very large value.



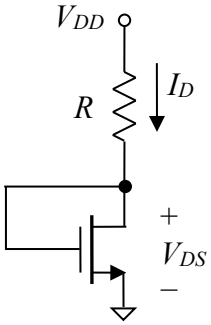
6. Shown to the right is a four-resistor bias network that has already been designed by assuming that the MOSFET has the nominal parameter values $k_n = 4.0\ mA/V^2$ and $V_t = 1.0$ V. Find the values of V_{GS} and V_{DS} under those conditions. Also determine how far (how many volts) the value of V_{DS} is above the saturation-triode boundary (defined by $V_{DS} = V_{GS} - V_t$). The "$V_{DD}/3$" rule-of-thumb has *not* been applied to this circuit to determine the values of R_D and R_S. The rule-of-thumb is not used when other constraints apply, so you can never assume that the voltages across R_D and R_S are equal to $V_{DD}/3$ unless it is explicitly stated somewhere that they are.



***Ungraded Problems*:**

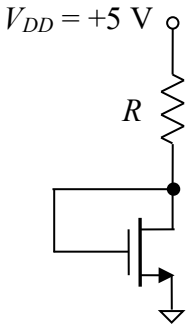
The following problems will not be graded, but you should attempt to solve them on your own and then check the solutions. Do not give up too quickly if you struggle with one or more of them. Move on to a different problem and then come back to the difficult one after a few hours.

1. Measurements are performed on an *n*-channel MOSFET in a test configuration like the one shown at right that has the gate shorted to the drain. It is found that the DC drain current is 0.40 mA for $V_{GS} = V_{DS} = 1.0$ VDC and 0.10 mA for $V_{GS} = V_{DS} = 0.80$ V. Use the measured data to estimate the values of k_n and V_t for the MOSFET. The tests assume that $\lambda = 0$ (i.e., there is no channel length modulation).

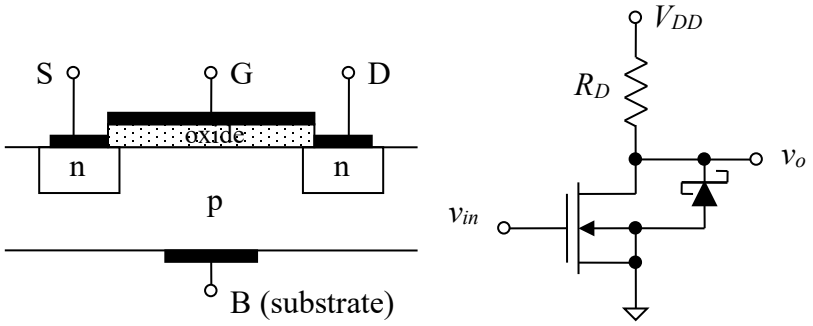


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2. The "diode-connected" NMOS device in the circuit shown to the right is fabricated using the 0.8 μm process. The approximate parameter values are $V_t = 0.70$ V, $L = 0.80$ μm (channel length), and $\mu_n C_{ox} = 130\ \mu\text{A/V}^2$. Find the required values for the channel width W and the resistance R to establish a drain-to-source voltage V_{DS} of 2.5 V and a drain current i_D of 3.0 mA. You may ignore the channel-length modulation effect (i.e., assume that $\lambda = 0$). *Hint*: It is impossible for a MOSFET to operate in one of the three regions of operation if it is diode-connected.



3. The diagram below left depicts the internal structure of an *n*-channel enhancement-mode MOSFET. In the diagram to the right, the same MOSFET is used in a basic inverter circuit. Also indicated in the circuit diagram is a Schottky diode that has been added between the substrate terminal and the drain terminal. MOSFET manufacturers often add Schottky diodes like this as protective measures, especially in CMOS circuits. Give a valid explanation for the presence of the diode in the circuit. An important point (and hint) is that Schottky diodes have lower turn-on voltages (approximately 0.3 V) than standard silicon *pn* junction diodes.



4. The lecture notes "Source Degeneration Biasing for Discrete MOSFET Amplifiers" present the derivation of the expression below for the quiescent drain current of a MOSFET with a four-resistor bias network.

$$I_D = \frac{V_G - V_t}{R_S} + \frac{1}{k_n R_S^2} - \frac{1}{k_n R_S^2}\sqrt{1 + 2k_n R_S (V_G - V_t)}$$

Show that this expression reduces to

$$I_D = \frac{1}{2} k_n (V_{GS} - V_t)^2$$

if $R_S \to 0$. Note that if $R_S = 0$, then in the circuit $V_G = V_{GS}$. *Hint*: If $R_S \to 0$, then the second term under the radical (square root) sign becomes much smaller than 1. There are Taylor series approximations available for the function $(1 + x)^{1/2}$ for $|x| << 1$. (You do not have to derive the Taylor series approximation, but feel free to do so if you are inspired!)

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5. As explained in Sec. 5.4.4 of the textbook (Sedra & Smith, 8th ed.), the MOSFET parameter values k'_n and V_{tn} are sensitive to temperature. (Recall that $k_n = k'_n\, W/L$ and that $k'_n = \mu_n C_{ox}$.) Both values decrease with rising temperature, but the changes have opposite effects on the drain current. The effects are present whether the MOSFET operates in the saturation region or the triode region, but their impacts are more obvious for the saturation case since the expression for i_D is simpler:

$$i_D = \frac{1}{2} k_n \left(v_{GS} - V_{tn} \right)^2 .$$

For a given value of v_{GS}, decreasing V_{tn} causes i_D to rise, whereas decreasing k_n causes i_D to fall. Because the change in V_{tn} is only about 2 mV/°C, the change in k_n usually dominates, so i_D usually decreases with increasing temperature in MOSFET circuits. However, if the overvoltage ($v_{GS} - V_{tn}$) is relatively small (less than a volt or so), then the change in V_{tn} can dominate, which causes i_D to rise with rising temperature. An example of the crossover from V_{tn} dominance to k_n dominance is Fig. 5 of the Fairchild Semiconductor 2N7000 datasheet available at the ECEG 350 Laboratory web page.

For the MOSFET circuit depicted to the right, assume that the overvoltage is large so that the temperature variation of V_{tn} can be ignored and that $V_t \approx 1.0$ V at all temperatures. Also assume that $\lambda = 0$. Suppose that $k_n = 1.0$ mA/V^2 initially but then the temperature decreases, which causes k_n to rise. Find the value of k_n at which the MOSFET makes the transition from the saturation region to the triode region. This type of temperature instability is greatly reduced if a source degeneration resistor (usually labeled R_S in Sedra & Smith) is added between the source terminal and ground.

