**ECEG 350 Electronics I Fall 2023**

**Homework Assignment #8 – due via Moodle at 11:59 pm on Friday, Nov. 10, 2023**

***Instructions, notes, and hints*:**

You may make reasonable assumptions and approximations in order to compensate for missing information, if any. Provide the details of all solutions, including important intermediate steps. You will not receive credit if you do not show your work.

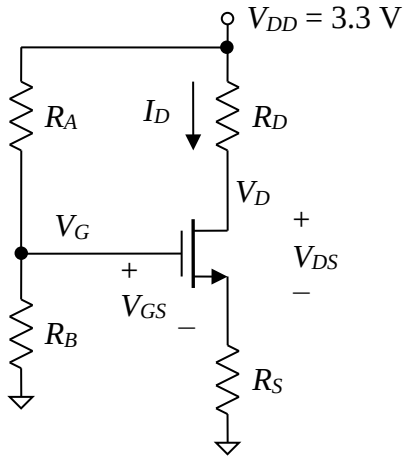
A good source of additional examples is the extensive Sec. 5.3 in the textbook (Sedra & Smith, 8th ed.).

***Graded Problems*:**

**1.** After a series of tests, it is found that the MOSFET in the four-resistor bias network shown below has a threshold voltage of $V_t = 0.8$ V and that the drain current is 500 μA when the device is operated in the saturation region with $v_{GS} = 1.2$ V. The measurement results help to determine the value of $k_n$. Assume that $\lambda = 0$ (i.e., no channel-length modulation).

**a.** Find the required resistor values so that $I_D = 300$ μA. Apply the standard rule-of-thumb that sets $I_D R_D = I_D R_S = V_{DS} = V_{DD}/3$, and choose the values of $R_A$ and $R_B$ so that $R_A \| R_B \geq 500$ kΩ. An infinite number of combinations of $R_A$ and $R_B$ values will work.

**b.** The designers discover that they need more "headroom" and "legroom" for the *total* node voltage $v_D$. (Headroom and legroom are the ranges of voltages over which $v_D$ can vary above and below the quiescent voltage $V_D$ to avoid operation in the cut-off and triode regions. The total range of $v_D$ is sometimes called the "swing range.") The designers therefore decide to make $I_D R_S = 0.25 V_{DD}$ (the voltage across $R_S$) while keeping $I_D$ the same. Find the required values of $R_A$, $R_B$, and $R_S$ to allow for the change. Also find the value of $R_D$ required to place quiescent node voltage $V_D$ at the midpoint between $I_D R_S$ and $V_{DD}$ (roughly equal headroom and legroom). The values of $R_A$ and $R_B$ should still be chosen so that $R_A \| R_B \geq 500$ kΩ.

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**2.** Shown on the next page is a common-source (CS) amplifier that uses four-resistor biasing. The load has an equivalent resistance of 2.5 MΩ, so it can be ignored for gain calculations. The circuit uses the biasing rule-of-thumb that sets $I_D R_D = I_D R_S = V_{DS} = V_{DD}/3$. The resulting quiescent drain current is around 1.0 mA, and the voltage gain is $A_v = v_o/v_{in} = -40$ V/V. The magnitude of the input voltage $v_{in}$ must be less than 40 mV to satisfy the small-signal condition (assuming that a factor of 1/10 corresponds to "much less than").

Higher gain can be achieved by distributing the quiescent voltages differently. Since $R_L >> R_D$,

$$A_v \approx -g_m R_D = -\sqrt{2k_n I_D}\,R_D = -\sqrt{2k_n I_D}\left(\frac{I_D R_D}{I_D}\right) = -\sqrt{\frac{2k_n}{I_D}}\left(I_D R_D\right),$$

which suggests that the gain of a CS amplifier can be increased by increasing the quiescent voltage across $R_D$ (i.e., the voltage $I_D R_D$) and/or decreasing the quiescent drain current. However, increasing the voltage $I_D R_D$ can push the quiescent point closer to the triode region unless the voltage across $R_S$ (the voltage $I_D R_S$) is reduced as well because, by KVL,

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S \quad \rightarrow \quad V_{DS} = V_{DD} - I_D R_D - I_D R_S,$$

and we need to maintain

$$V_{DS} > V_{GS} - V_t = V_{OV}.$$

Remember that the *total* voltage $v_{DS}$ fluctuates if a signal is present, so the *bias* value $V_{DS}$ must be comfortably above $V_{OV}$. Reducing the voltage across $R_S$ results in less stable bias conditions, so this approach represents a trade-off. If the value of $I_D$ is reduced to increase the gain, then the small signal condition becomes more constrained because

$$I_D = \frac{1}{2}k_n\left(V_{GS} - V_t\right)^2 = \frac{1}{2}k_n V_{OV}^2 \quad \rightarrow \quad V_{OV} = \sqrt{\frac{2I_D}{k_n}} \quad \text{and} \quad \left|v_{gs}\right| << 2\left(V_{GS} - V_t\right) = 2V_{OV}.$$

That is, a smaller $I_D$ leads to a smaller $V_{OV}$, which in turn leads to a tighter restriction on the magnitude of $v_{gs}$, which in the CS amplifier below is equal to the small-signal voltage $v_{in}$.

Suppose that the designers of the amplifier below decide to increase the gain by increasing the voltage across $R_D$ to $0.4V_{DD}$ and decreasing the voltage across $R_S$ to $0.26V_{DD}$ to compensate. They will also reduce $I_D$ from 1.0 mA to 500 μA. Find:

- **a.** the new values of $R_A$, $R_B$, $R_D$, and $R_S$ to meet the new specifications
- **b.** the new voltage gain $A_v = v_o/v_{in}$. Use a small-signal model for your analysis.
- **c.** the new limit on the input voltage magnitude $|v_{in}|$, assuming that a factor of 1/10 corresponds to "much less than"

The MOSFET's parameters are $k_n = 50$ mA/V$^2$ and $V_t = 2$ V. All of the capacitors have negligible reactances at the signal frequency.

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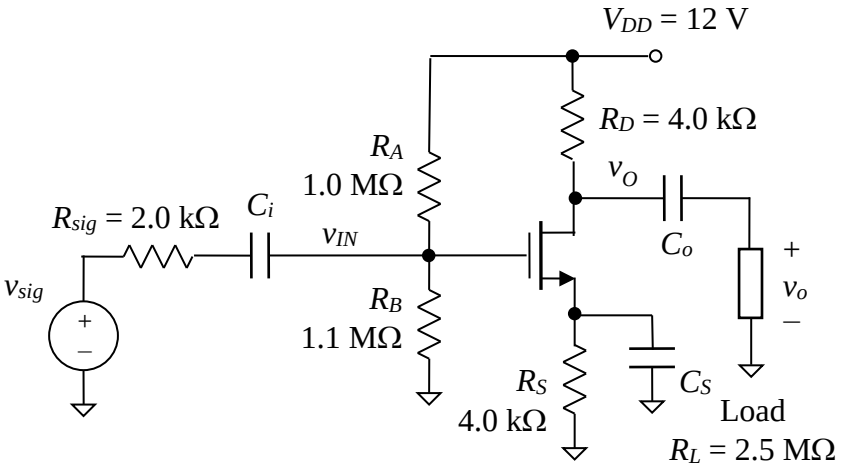
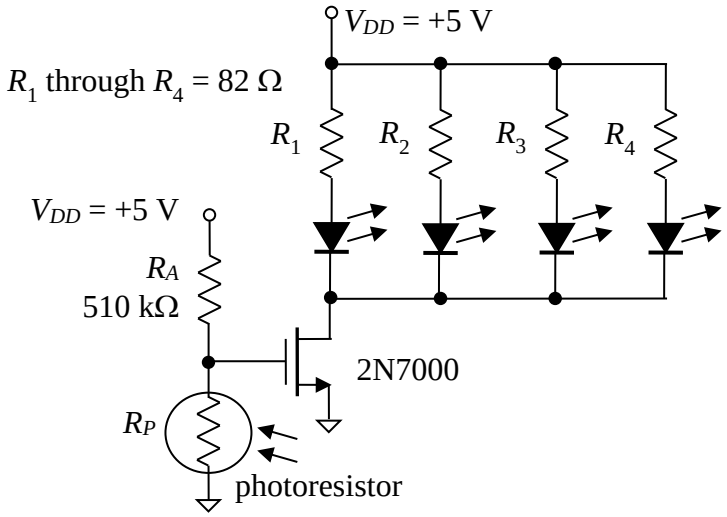



**Circuit diagram for Prob. 2.**

**3.** As shown below, a 2N7000 MOSFET is used to switch four white LEDs on or off depending on the state of a photoresistor $R_P$. The resistance of $R_P$ varies from around 300 Ω in bright conditions to around 3 MΩ in the dark. Assuming that all of the LEDs are identical and have turn-on voltages of 3.2 V, find the region of operation and the drain-to-source voltage of the 2N7000 when the light conditions are such that $R_P$ = 1.2 MΩ. Also find the power dissipation of the MOSFET in this state. Assume that $V_t$ = 2.1 V and $k_n$ = 200 mA/V$^2$ for the 2N7000. The 2N7000 data sheet is available at the ECEG 350 Laboratory web page.

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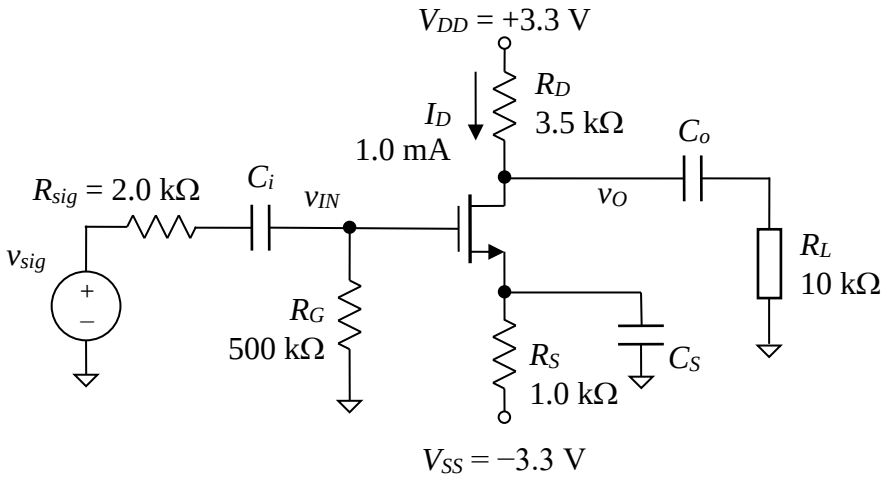
**4.** The n-channel MOSFET in the circuit shown below has $k_n$ = 800 μA/V$^2$ and $V_t$ = 0.70 V. The circuit uses a bipolar (±3.3 V) power supply. The resistor values have been chose to produce a quiescent drain current $I_D$ of 1.0 mA and a quiescent value for $V_{DS}$ that is 0.50 V above the triode-saturation boundary (defined by $V_{DS} = V_{GS} - V_t$). Assuming that $\lambda = 0$ (i.e., that there is no channel-length modulation), find the small-signal voltage gain $v_o/v_{in}$ of the amplifier. Use a small-signal model for your analysis. You may assume that all three capacitors have negligible reactance over the operating frequency range of the amplifier.




***Ungraded Problems*:**

The following problems will not be graded, but you should attempt to solve them on your own and then check the solutions. Do not give up too quickly if you struggle with one or more of them. Move on to a different problem and then come back to the difficult one after a few hours.

**1.** The lecture notes "Source Degeneration Biasing for Discrete MOSFET Amplifiers" present the derivation of the expression below for the quiescent drain current of a MOSFET with a four-resistor bias network.

$$I_D = \frac{V_G - V_t}{R_S} + \frac{1}{k_n R_S^2} - \frac{1}{k_n R_S^2}\sqrt{1 + 2k_n R_S (V_G - V_t)}$$

Show that this expression reduces to

$$I_D = \frac{1}{2} k_n (V_{GS} - V_t)^2$$

if $R_S \to 0$. Note that if $R_S = 0$, then in the circuit $V_G = V_{GS}$. *Hint*: If $R_S \to 0$, then the second term under the radical (square root) sign becomes much smaller than 1. There are Taylor series approximations available for the function $(1 + x)^{1/2}$ for $|x| << 1$. (You do not have to derive the Taylor series approximation, but feel free to do so if you are inspired!)

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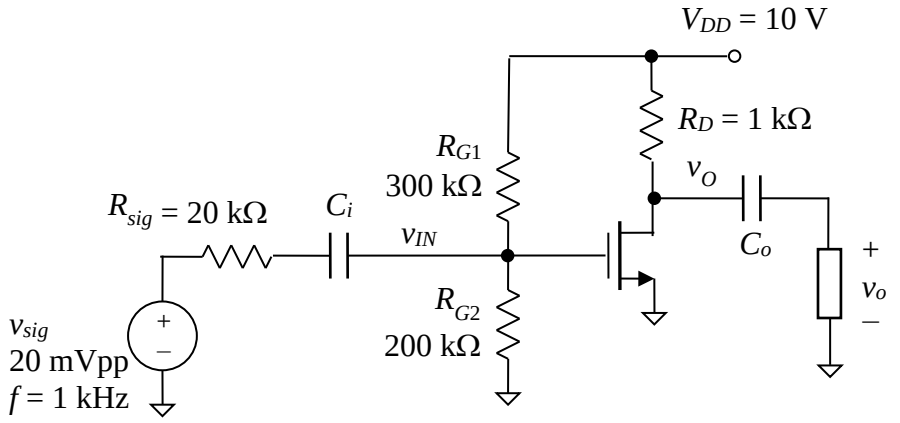
**2.** The common-source amplifier circuit shown below is not practical because there is no source degeneration resistor to stabilize the bias voltages and currents. However, some insights into amplifier operation can be gained from it. A sinusoidal signal $v_{sig}(t)$ with the indicated properties is applied to the input. (The phase doesn't matter, so assume that it is zero.) The MOSFET has the parameter values $k_n$ = 1.0 mA/V$^2$ and $V_t$ = 1.0 V. Since this is an amplifier, you may assume that the designers intended for the MOSFET to operate in the saturation region at all times. You may also assume that $\lambda = 0$, that all of the capacitors have negligible reactances at the signal frequency, and that the load acts like an open circuit.

- **a.** Use an appropriate small-signal model of the circuit to find the numerical value of the small-signal voltage gain $A_v = v_o/v_{in}$, assuming linear operation around the quiescent point.
- **b.** Suppose that the values of resistors $R_{G1}$ and $R_{G2}$ are changed so that the quiescent gate-to-source voltage $V_{GS}$ is just barely above the threshold voltage $V_t$ (i.e., the MOSFET is on the edge of the cut-off region). Find the value of the small-signal voltage gain $A_v$ at the new operating point.
- **c.** Now suppose that the quiescent gate-to-source voltage $V_{GS}$ has the value that causes the MOSFET to operate at the boundary between the saturation and triode regions, that is, at point B in Fig. 7.2b of Sedra & Smith, 7th ed. Find the small-signal voltage gain value for this case.

Note that in practice the amplifier should not be operated in either of the conditions represented by parts b and c because the output voltage has no room to swing above and below its quiescent value without the MOSFET entering the cut-off (part b) or triode (part c) region. The voltage gains found in the two parts represent theoretical lower and upper limits for this particular circuit.




**3.** Measurements are performed on an *n*-channel MOSFET in a test configuration that has the gate shorted to the drain. It is found that the DC drain current is 0.40 mA for $V_{GS} = V_{DS}$ = 1 .0 VDC and 0.10 mA for $V_{GS} = V_{DS}$ = 0.80 V. Use the measured data to estimate the values of $k_n$ and $V_t$ for the MOSFET. The tests assume that $\lambda = 0$ (i.e., there is no channel length modulation).