Homework Assignment #8 – due via Moodle at 11:59 pm on Tuesday, December 9, 2025
[Prob. 4b revised 12/6/25; extended deadline]

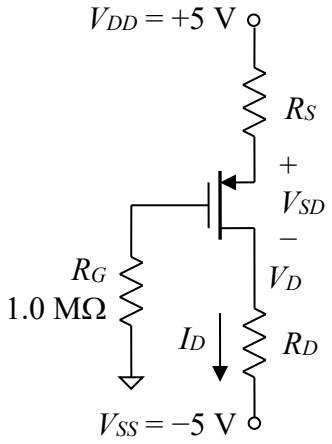
***Instructions, notes, and hints*:**

You may make reasonable assumptions and approximations to compensate for missing information, if any. Provide the details of all solutions, including important intermediate steps. You will not receive credit if you do not show your work.

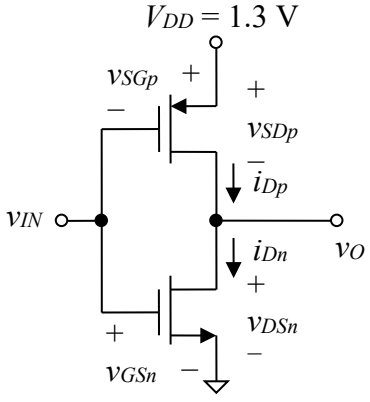
The first few problems will be graded and the rest will not be graded. Only the graded problems must be submitted by the deadline above. Do not submit the ungraded problems.

***Graded Problems*:**

1. The circuit shown at right is driven by a bipolar power supply with ±5 V. The PMOS device has the parameter values $V_t = -1.5$ V, $k_p = 30$ mA/V^2, and $\lambda = 0.020$ V^{-1}. The value of R_G has already been set. Find the values of R_S and R_D that result in a DC bias current of 2.5 mA and that cause the MOSFET to operate in the saturation region with a quiescent drain voltage that is 1.5 V away from the saturation-triode boundary. Ignore the channel-length modulation effect. *Hint*: $V_{SD} > V_{SG} - |V_{tp}|$, which implies that $V_D < V_G + |V_{tp}|$. (Why?)



2. The MOSFETs in the CMOS inverter circuit depicted below are matched, which means that $V_{tn} = |V_{tp}|$ and $k'_n(W_n/L_n) = k'_p(W_p/L_p)$. Consequently, the circuit has the voltage transfer characteristic shown in Fig. 16.25 of Sedra & Smith, 8th ed. Suppose that the input makes a transition over a short period of time from logical 0 to logical 1 so that the input voltage v_{IN} increases from 0 V to V_{DD}. The load connected to the v_O terminal draws negligible current.



a. The drain currents (which are equal) have their maximum value at the instant when $v_{IN} = 0.5V_{DD}$, which causes both FETs to operate in the saturation region. Find the numerical value of the peak current for $V_{tn} = |V_{tp}| = 0.4$ V, $k'_n = 500$ μA/V^2, $(W_n/L_n) = 1.5$, and $V_{DD} = 1.3$ V. The values of k'_p and (W_p/L_p) are determined by the transistor matching condition; assume that $\mu_p = 0.25\mu_n$.

b. Find the upper limit V_{IL} of logic level 0 input voltages and the lower limit V_{IH} of logic level 1 input voltages. Also find the associated low-input noise margin NM_L and high-input noise margin NM_H. Compare them to the ideal value of $0.5V_{DD}$.

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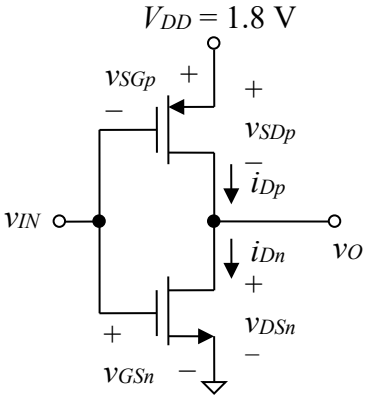
3. A CMOS inverter like the one depicted below will be fabricated using the 0.18-μm process. The various parameter values are given in the MOSFET process technology table that can be found in Appendix K of the textbook (Sedra & Smith, 8th ed.) or at the course Moodle site in the "Additional Resources" section. The power supply will have the recommended value of V_{DD} = 1.8 V, and both MOSFETs will have a channel length of 0.18 μm. The load connected to the v_O terminal draws negligible current.

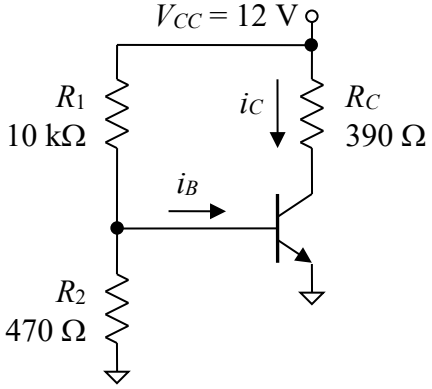


- **a.** Assuming that W_n/L_n = 2.5 for the NMOS device, find the required channel width W_p of the PMOS device so that $V_M = V_{DD}/2$, that is, so that the vertical part of the curve in the voltage transfer characteristic is halfway between v_{IN} = 0 V and $v_I = V_{DD}$ (as shown in Fig. 16.25 of the textbook).
- **b.** Find the total area under the gate terminal (in μm^2) for each MOSFET for the width W_p found in Part **a**.
- **c.** For the width W_p found in Part **a**, find the output resistance of the inverter for each of the two input states (i.e., for logical input 0 and logical input 1).

4. Suppose that you have found a CMOS inverter that was fabricated using the now very-old 0.8-μm process. It is intended to operate with a 5-V power supply. The various parameter values are given in the MOSFET process technology table that can be found in Appendix K of the textbook (Sedra & Smith, 8th ed.) or at the course Moodle site in the "Additional Resources" section.

- **a.** Assuming that the NMOS and PMOS devices are matched, find the maximum permitted logical 0 level at the input V_{IL} for inverters made with the 0.8-μm process.
- **b.** **[text in boldface added 12/6/25]** Suppose that the inverter is driving other CMOS inverters connected to its output terminal. When the output of the inverter transitions from a logical 1 to a logical 0, the charge stored in the gate capacitance of the "downstream" logic gates will flow into the output terminal of the inverter. Thus, the inverter must be able to "sink" current at its output. The sink current flows through the output resistance of the NMOS device to ground. Given the result found in Part **a**, estimate the maximum current that the output terminal of the inverter can sink while still producing an output voltage that can be considered "low" for the following inverters. **Assume that W_n/L_n = 1.5.**

5. Explain why the silicon *npn* BJT in the diagram to the right operates in the cut-off region. Assume that the turn-on voltage V_F of the base-emitter junction is 0.7 V and that $V_{CE}|_{sat}$ = 0.2 V. The β value of the BJT ranges from 100 to 300 depending on temperature and manufacturing variability.



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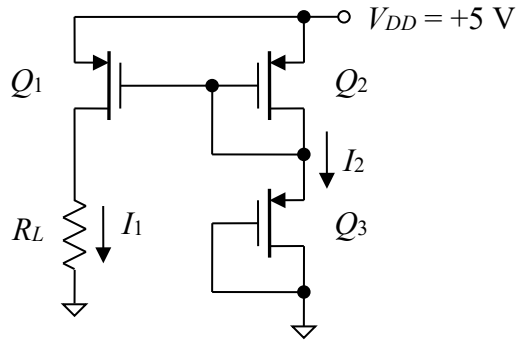
***Ungraded Problems*:**

The following problems will not be graded, but you should attempt to solve them on your own and then check the solutions. Do not give up too quickly if you struggle with one or more of them. Move on to a different problem and then come back to the difficult one after a few hours.

1. The circuit shown below is called a *current mirror* because it is designed to cause the current I_1 flowing through the load represented by resistance R_L to be the same as current I_2, the value of which is determined by adjusting the dimensions of Q_2 and Q_3. In effect, the circuit acts like an almost ideal current source for the load. (The channel-length modulation effect and other practical limitations keep it from being ideal, but you may ignore channel-length modulation here.) All three PMOS devices are fabricated on the same silicon die with $\mu_p C_{ox}$ = 58 μA/V^2, L = 800 nm, and $V_t \approx -0.7$ V. Transistors Q_1 and Q_2 both have channel widths of 2.16 μm. You may assume that $\lambda = 0$ and that Q_1, Q_2, and Q_3 are all operating in the saturation region, which is a necessary condition for the circuit to operate properly. Current mirrors are often used to establish controlled bias currents in integrated circuit amplifiers.

- **a.** Find the required channel width of Q_3 so that the load current I_1 is equal to 50 μA. Show why $I_1 = I_2$ (a very simple proof).
- **b.** Because Q_2 and Q_3 are in the so-called diode-connected configuration (so that $v_{SD} = v_{SG}$), they always operate in the saturation region if they are not cut off. Find the range of values of R_L for which Q_1 also operates in the saturation region.
- **c.** Explain how the width W_1 of Q_1 could be altered, and by how much, so that $I_1 = 3I_2$. The widths of Q_2 and Q_3 would remain unchanged.



2. Equations (16.37) and (16.38) in the textbook (Sedra & Smith, 8th ed.) give the high-input and low-input noise margins for a CMOS inverter in which the MOSFETs are matched in the sense that $V_{tn} = |V_{tp}|$ and $k'_n(W_n/L_n) = k'_p(W_p/L_p)$. Recall from Sec. 16.2.3 of the textbook that an ideal inverter would have $NM_L = NM_H = 0.5V_{DD}$. Find the common value of the threshold voltage magnitude V_t that both the NMOS device and the PMOS device must have to achieve ideal noise margins. *Note*: Given that the value of V_t cannot be set with high precision using current fabrication methods, the value of V_t in practical inverter circuits is substantially lower than the "ideal" value that would yield $NM_L = NM_H = 0.5V_{DD}$. As explained in Chap. 17 of the textbook, high V_t values, especially those approaching the "ideal" value, lead to greatly reduced switching speeds between logical states.

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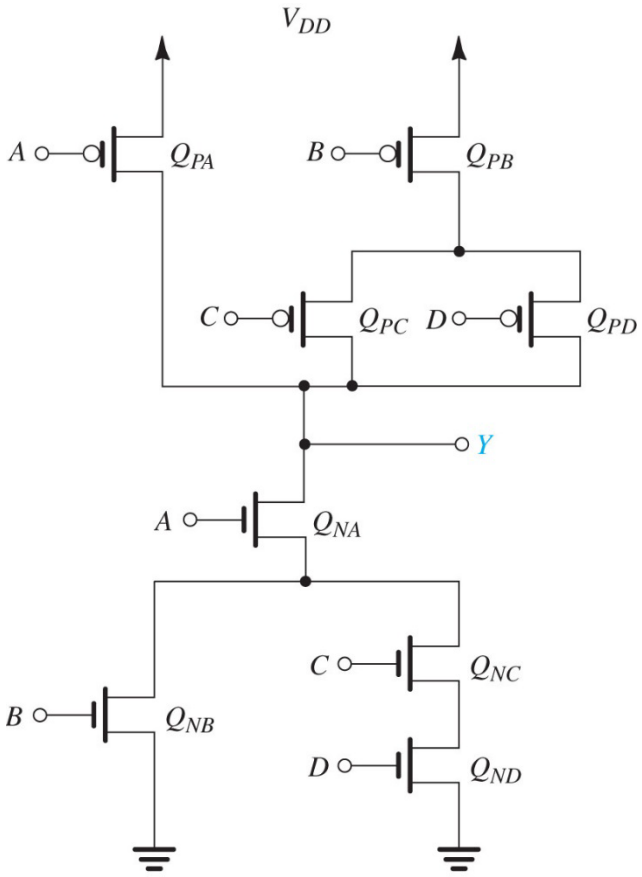
3. Shown below is a complicated CMOS logic gate that implements the Boolean operation indicated by the expression below the gate. The diagram is Fig. 16.9 of the textbook (Sedra & Smith, 8th ed.) The PMOS and NMOS devices are represented using a common pair of alternate symbols. The four MOSFETs in the upper half of the diagram (with "*P*" in the subscripts) are PMOS devices, and the four in the lower half of the diagram (with "*N*" in the subscripts) are NMOS devices. Note that the PMOS device symbols have small circles next to their gates while the NMOS device symbols do not. All four PMOS devices are "flipped;" that is, their source terminals are on the upper side of their respective symbols. Find the region of operation of each of the four PMOS devices for the following binary input combinations, and explain why the total current through the circuit is zero in each case.

a. ABCD = 0110
b. ABCD = 1100



$Y = \overline{A(B + CD)}$