

Lab #1: Input Offset Voltage and Bias Current Measurements

Introduction

Operational amplifiers are widely used in analog design because their very high gain controlled by negative feedback leads to simple circuits with predictable and reliable performance. However, non-ideal characteristics such as input offset voltage and input bias currents call for special design techniques in precision applications. In this two-week lab exercise, you will determine the input offset voltage and input bias currents of a common type of op-amp and develop a sense of the extent of their effects in typical circuits. Group assignments are listed at the end of this handout.

Theoretical Background

An ideal op-amp has zero current flowing into its input terminals and a virtual short between the terminals when negative feedback is present. However, because it is impossible to manufacture op-amps with infinite open-loop gain, perfectly symmetrical input circuitry, and zero input current, a more realistic model of the op-amp such as the one shown in Figure 1 is sometimes required to account for these limitations. The DC voltage source V_{OS} models the input offset voltage, and the two DC current sources I_{B1} and I_{B2} model the input bias currents. In general, $I_{B1} \neq I_{B2}$, but they are usually close in value.

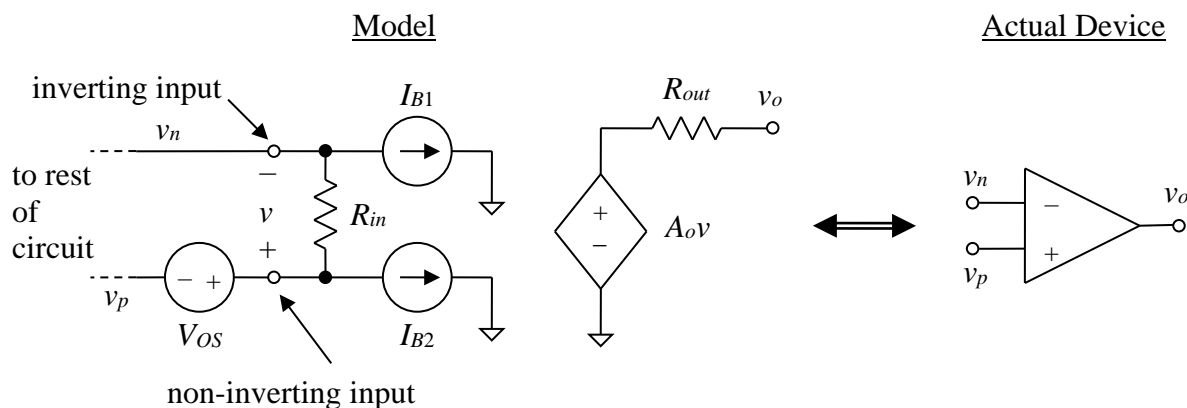


Figure 1. Circuit model of op-amp that includes input offset voltage V_{OS} and input bias currents I_{B1} and I_{B2} . Note that voltage source V_{OS} is modeled outside the op-amp's terminals but can be placed in series with either terminal. The polarity of the source is not important because V_{OS} could be positive or negative in value. The sources I_{B1} , I_{B2} , and V_{OS} are DC sources and are completely independent from the signal source (often modeled by a voltage source v_{in}).

In almost all applications it is safe to assume that $R_{in} \rightarrow \infty$ and $R_{out} = 0$, but it is not uncommon for the offset voltage and bias currents to cause problems in practical circuits. Therefore, being

able to compensate for these imperfections is an important design skill, and this in turn requires knowledge of the range of values to expect. While it is usually sufficient to obtain this information from a data sheet, in some cases more exact measurements are required, a data sheet might not be available, or the data sheet is incomplete.

Experimental Procedure

Complete the following steps with your lab partners:

- Devise a set of test circuits and an accompanying set of measurements from which you can determine the values of the input offset voltage V_{OS} and the input bias currents I_{B1} and I_{B2} for a single op-amp. Because all three effects are present simultaneously, you will have to use three different test circuits to highlight each one. It is also possible, maybe even likely, that you will have to solve a system of equations constructed from your measured data to extract the desired quantities because the output voltage is likely to depend on two or more of them.

Several possible test circuits are shown in Figure 2. You do **not** have to use any or all of them. You may replace them with different circuits if your group devises a different approach. Determine resistor or capacitor values (or both) that are appropriate for the expected approximate values of the quantities that you are trying to measure. For the circuits shown in Figure 2b and 2d, it might be helpful to recall the relationships

$$i = C \frac{dv}{dt} \rightarrow \frac{dv}{dt} = \frac{i}{C} \rightarrow v(t) = v(t_o) + \frac{1}{C} \int_{t_o}^t i(\tau) d\tau .$$

Note that none of the circuits in Figure 2 has an input voltage indicated because they are test circuits, not amplifiers. The input sources for these circuits are the input offset voltage and the input bias currents. Your goal is to determine the values of V_{OS} , I_{B1} , and I_{B2} by observing their combined effects on the output voltage v_o in each circuit and then devising some method to isolate their values. Thus, you will need to measure and record v_o in each circuit using either a multimeter (if v_o is expected to be DC) or an oscilloscope (if v_o is expected to vary with time). Again, remember that all three sources are active simultaneously in any given test circuit, and all of them can contribute to v_o .

It is likely that both the multimeter and the oscilloscope will be subject to noise that will cause measurement uncertainties on the order of at least a few millivolts. Some of the noise is due to phenomena that we will not cover in this course. You should therefore design test circuits that are likely to produce output voltages of several tens of millivolts or more in response to the expected values of V_{OS} , I_{B1} , and I_{B2} so that noise has only a minor effect on your measurements. That is, the effects of V_{OS} , I_{B1} , and/or I_{B2} should “drown out” the noise.

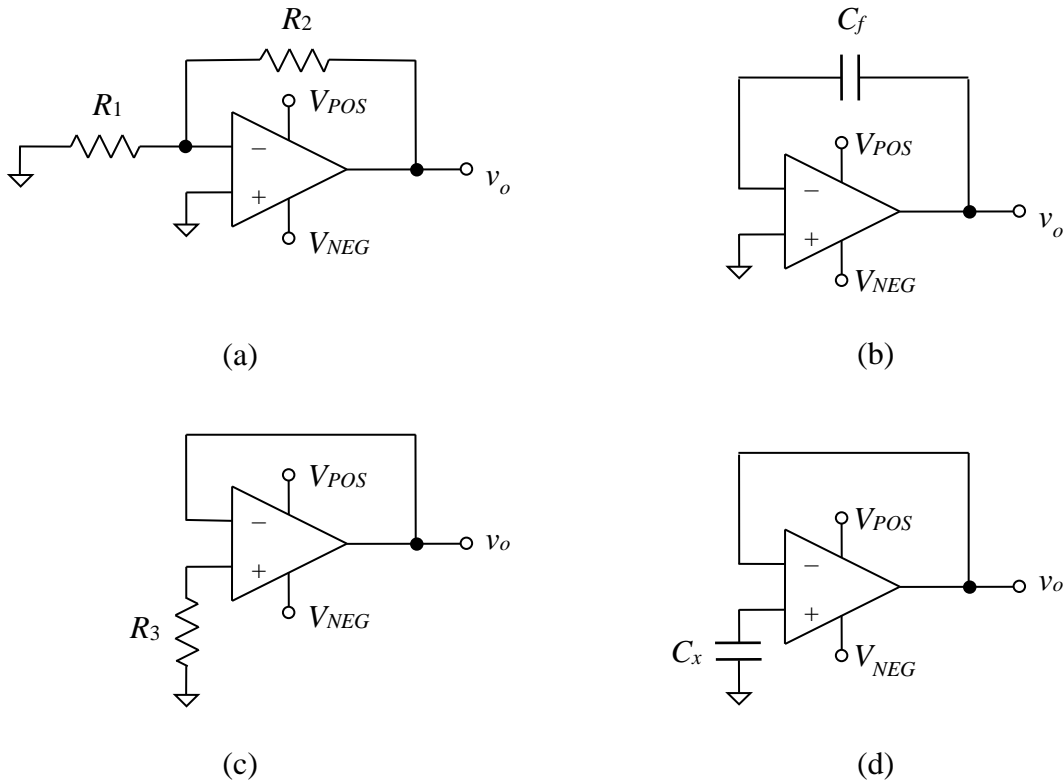


Figure 2. Test circuit configurations that could be used to help determine the values of V_{OS} , I_{B1} , and I_{B2} for a given op-amp. Note that these are not practical circuits for typical applications. Node voltages V_{POS} and V_{NEG} in the diagram represent the power supply voltages. The “COM” terminal of the power supply should be connected to the ground node.

- Read the following important hints and items of advice. They could save you a lot of time:
 1. Keep good records of your test procedures since you will most likely have to refer back to earlier measurements during the lab session and while you complete your post-lab activities. You also want to avoid repeating mistakes. Organize your data!
 2. Because the values of V_{OS} , I_{B1} , and I_{B2} are different between individual op-amps, **all measurements should be made on the same op-amp**. You are therefore strongly encouraged to build three separate test circuits and move the op-amp between them. In the past, a lot of demonstration time was wasted while students rebuilt their test circuits, which often led to failures because construction was rushed.
 3. Use the same power supply voltages V_{POS} and V_{NEG} for each test circuit. Some of the quantities that you are trying to measure vary with the applied power supply voltage.
 4. Model V_{OS} the same way in each test circuit. Always give it the same polarity, and place it in series with the same input terminal of the op-amp. If you have to solve a set of simultaneous equations, the polarity and location of V_{OS} will need to be consistent from one circuit to the next. Remember also that I_{B1} and I_{B2} always flow into the op-amp’s terminals.

5. Keep in mind practical limitations such as the tolerances of the components and how they might affect measurement accuracy. Electrolytic capacitors can have tolerances up to 40% or more, and the tolerance is often not symmetrical about the labeled value.
 6. It is very difficult to measure voltages smaller than roughly 10 mV accurately using the equipment available in the ECE labs, primarily because of the presence of noise.
 7. You are trying to highlight, not mitigate, the various DC imperfections so that you can measure them. Thus, you should *not* apply the offset voltage or bias current mitigation techniques discussed in class and in the textbook.
 8. Keep resistor values within a reasonable range. Avoid very small values since they could lead to excessive current being drawn from the output terminal of the op-amp. You should also avoid resistor values above 8–10 M Ω or so since accumulated oil and dirt on the protoboard could create a bypass path with a comparable but indeterminate resistance value.
 9. Although not shown in Figure 2, you should connect bypass capacitors between each power supply pin (V_{POS} and V_{NEG}) and ground to help filter out some of the noise present on the power supply leads. A value of 10 μ F or so should help with low-frequency noise (like 60 or 120 Hz power supply ripple), but if WVBU seems to be a problem, try adding a capacitor of a few hundred picofarads in parallel with each large bypass capacitor. High-frequency bypass capacitors should be mounted as close to the IC as possible using short leads. Electrolytic capacitors are ineffective in the bypassing role at radio frequencies because they act more like inductors or large complex impedances in that range.
 10. Pay attention to the polarity of electrolytic capacitors, especially the one placed in parallel with the negative power supply!
 11. If noise pick-up on the multimeter's test leads prevents you from obtaining reliable voltage measurements, try to reduce the effect by twisting the leads together. Try twisting the power supply leads to the circuit as well. That is, form twisted pairs when possible. For the bipolar power supply, which has three leads (+, –, and COM), try braiding the leads.
- After you have devised a test procedure, perform a “pencil-and-paper” analysis of each test circuit with typical values for V_{OS} , I_{B1} , and I_{B2} taken from the op-amp's datasheet to get an idea of the procedure's effectiveness. Again, each individual test circuit should highlight only one of the DC imperfections, or the circuit measurements taken together should lead to a system of equations that can be solved with a high degree of confidence in the results. Each imperfection should be accentuated in at least one of the test circuits. In some cases, it might be possible to accentuate one of the imperfections enough in a particular circuit to render negligible the effects of the others. Make any necessary modifications before proceeding.
 - When you are satisfied with the test procedure that you have devised, obtain an op-amp, and use your procedure to determine the values of V_{OS} , I_{B1} , and I_{B2} . Compare the values that you calculate to the typical and maximum values listed in the datasheet for the device. Keep your hands and fingers away from the circuit while you are making measurements. Stray capacitance sometimes affects the readings. (Try it!) If your original test procedure does not work well, keep modifying it until it does. One test of the validity of your results is to compare the values of I_{B1} and I_{B2} that you obtain. Both values should be positive (i.e., the currents flow into the op-amp's terminals), and they should be fairly close to each other (a difference of much less than 40–50% or so).

- When you are confident that your test configuration is working properly, schedule a post-lab meeting (length up to 30 min) with me at a mutually agreed time before the deadline posted on the Laboratory page at the course web site. The following guidelines apply:
 - All group members must be present.
 - The meeting will take place in the Maker-E if Dana 307 is not available at the scheduled time.
 - Meetings will be scheduled in the order that requests are received.
 - Meetings will not be rescheduled if the first one reveals circuit problems, wiring failures, errors in the test procedure, or a lack of preparation.
 - Deadline extensions will generally be approved for confirmed illnesses or other extenuating circumstances.
 - Preparation instructions are given in the “Post-Lab Meeting” section below. **Read them carefully!** Note that you will need to prepare a set of visual aids to refer to during the meeting.

The visual aids that you intend to use must be combined into a single PDF document and **e-mailed** to me before the post-lab meeting begins. Use a file name of the form

“LName1_LName2_LName3_Lab1_fa23.pdf,”

where “LName1,” “LName2,” and “LName3” are the group members’ last names. Include the underscore (_) characters. For example, if students Alvarez, Chang, and Smith are lab partners, then their Lab #1 documentation would have the file name

Alvarez_Chang_Smith_Lab1_fa23.pdf

If your group has four members, then the file name should incorporate four last names instead of three. **The file size must be less than 5 MB.** Keep a copy of your documentation if you wish to use it to prepare for the next exam or need it for future reference.

Post-Lab Meeting

The purpose of the post-lab meeting will be to explain and demonstrate your measurement procedure. Each group member must describe the design and operation of one of your three test circuits and possibly answer a few follow-up questions. If your group has four members, then one person must explain the overall test procedure and how the measurements made with the three circuits tie together. Your group may decide how the various roles are assigned. Each person will have a time limit of about **five minutes** to respond.

Each person describing a test circuit must:

1. Make use of supporting visual aids (hand drawn is fine) that include the test circuit diagram with component values clearly labeled, all relevant equations, and any other graphics that might be helpful. All visual aids must be well organized, legible, and readily accessible to facilitate a lucid explanation. Leave out extraneous text, diagrams, and equations. Include only items that help explain how the circuit operates. Imagine that you are explaining your work to an immediate supervisor (not a vice president or client).

2. Briefly but concisely explain why this particular circuit was chosen, how the applicable equation was derived, and how the component values were selected to highlight one or more of the quantities being measured (V_{OS} , I_{B1} , and/or I_{B2}).
3. Successfully measure the test circuit's output voltage and demonstrate how the measured results are used in the applicable equation to contribute to an overall solution. This could be a simple voltage measurement using the multimeter, a time-domain measurement using the oscilloscope, or some other type of measurement.

In a four-person group, the fourth person must:

4. Make use of supporting visual aids (as described in requirement #1 above) to explain how the measurements from all three circuits are combined to determine the values of V_{OS} , I_{B1} , and I_{B2} . Also explain how you made sure that each quantity was accentuated (dominant) in at least one of the test circuits and how you accounted for the simultaneous presence of all three nonideal effects in the measurements. The measured values of V_{OS} , I_{B1} , and I_{B2} must then be compared to the expected values given in the op-amp's datasheet.

In a three-person group, requirement #4 above must be addressed by the group as a whole. The group may choose one spokesperson to present this part or involve everyone.

After the individual responses, there could be some general discussion of your design process and measurements, the performance characteristics of your circuits, how you handled any uncertainties, how you ensured the reliability of your calculations, and other related topics. If you made unusual design choices, you must be prepared to defend them.

Your group's lab score will be based on the effectiveness and accuracy of the test procedure, the extent to which each group member understands it, and the quality of your visual aids. It will be challenging to achieve a perfect score. A good demonstration must have excellent oral and visual components as well as technical accuracy.

Lab Scoring Criteria

Each group member will receive a score based on the following criteria quantized at the indicated levels. The first two criteria constitute a group base score; that is, each group member will receive the same score for those criteria. The score for the remaining criteria will be assessed independently and will be determined by that person's contribution to the post-lab meeting. The rubrics posted on the Laboratory page at the course web site will guide the assignment of scores. You should review it carefully to help you prepare for the post-lab meeting.

0, 8, 15, 23, 30 pts	Functionality of test circuits w/appropriate component values (group)
0, 8, 15, 23, 30 pts	Effectiveness of overall test procedure (group)
0, 8, 15, 23, 30 pts	Quality and accuracy of test circuit description (indiv.)
0, 2, 5, 8, 10 pts	Quality and effectiveness of supporting visual aids (indiv.)

If the meeting is completed after the deadline, a 10% score deduction will be applied for every 24 hours or portion thereof that it is late (not including weekend days) unless extenuating circumstance apply. No credit for the two individual criteria will be given four or more days after

the deadline; however, up to 60 pts will be assigned to each member of the group for the first two (group) criteria if at least one group member demonstrates the measurement procedure within a week of the deadline.

Group Assignments

The randomly generated groups for this lab exercise are listed below:

Baganski-Beebe-Zhang

Flynn-Jiorle-Rehman

Freedenberg-Powick-Ren

Beaudette -Samuels-Youn

Andrews-Ashnault-Regec

Bailey- Piper-Sagoe

Hackett-Jeong-Miller-Tuncel

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