Lab #4: MOSFET Bias Design and Amplifier Analysis

Introduction

Biasing is the process of selecting component values in a transistor circuit so that the proper quiescent (DC average) voltages and currents are established to meet a set of design goals. It is a key step in the design of amplifier circuits and some other types of circuits. A frequent requirement is to set and keep the quiescent voltages and currents close to target values despite variations in device parameters. In other situations, the exact values of the voltages and currents are not so important, but their stability relative to temperature changes or other environmental variations *is* important. In this lab exercise, you will design, assemble, test, and compare two types of MOSFET bias circuits. You will then use the more stable circuit as the basis of an amplifier and observe some of its performance characteristics. Group assignments are listed at the end of the handout. Note that there is one required in-lab demonstration described in the middle of p. 3.

Experimental Procedure

- **Read and study** the lecture notes "Source Degeneration Biasing for Discrete MOSFET Amplifiers," which is available at the course Moodle site. It will be difficult to complete the design procedure below without the information summarized in the notes.

- Design a four-resistor bias circuit like the one shown in Figure 1 for a 2N7000 *n*-channel enhancement-mode MOSFET (i.e., find values for R_D, R_S, R_A, and R_B). Bias control is usually used in amplifier circuits. Thus, you may assume that the specifications below apply when the MOSFET operates in the saturation region. The design specifications are listed at the top of the next page.

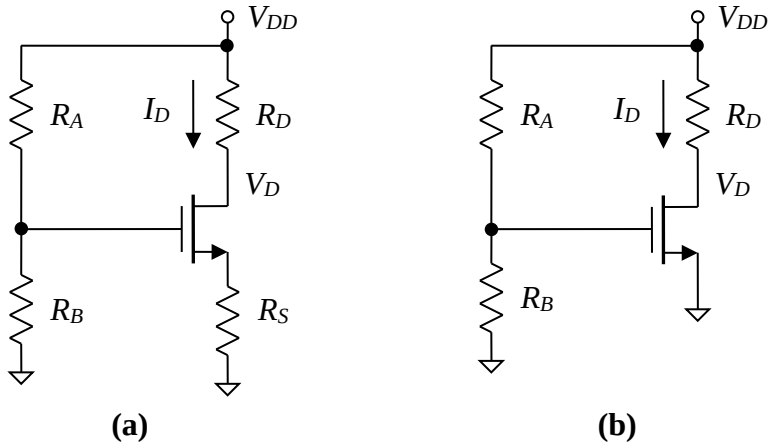

Figure 1. MOSFET biasing circuits that (a) uses a source degeneration resistor R_S or (b) fixes the value of the gate-to-source voltage.

Bias design specifications:

Power supply voltage V_{DD}: 15 V
Quiescent drain current I_D: 2.5 mA ± 0.3 mA
Quiescent drain voltage V_D: 10 V ± 1 V
Ensure that the current that flows through R_A and R_B is negligible compared to I_D, but do not use excessively large values for R_A and R_B; A single resistor with a value greater than 5–10 MΩ is too large.

Carefully review the notes and additional requirements listed below:

1. Information available on the 2N7000 MOSFET datasheet leads to the estimated parameter values V_t = 2.1 V and k_n = 200 mA/V^2. You may base your design on these nominal values. Note, however, that the actual values for the device you will use could differ considerably from the estimated values. There is no way to know what the actual values are unless you measure them, but a design based on nominal values is a valid approach if the potential errors are bounded in a known way and sufficiently small. It can be shown that this is the case for this type of bias design.
2. The design problem is not fully constrained, so many combinations of resistor values will meet the specifications. You will therefore have to make some design choices. Consider factors such as the current drain on the power source, reliability, the input resistance of the circuit if used as part of an amplifier, etc.
3. Only one physical resistor may be used for each resistance in the circuit unless multiple resistors are necessary to avoid exceeding power dissipation limits. In the latter case, each resistor in a series or parallel combination must have the same value.
4. All resistors must have values in the E24 series (standard values with 5% tolerance). Refer to the "Table of Standard Resistor Values" available at the ECEG 350 web site. Please contact me if a standard value that you need is not available in the lab parts bins.
5. Ensure that the power dissipation limits for the MOSFET and the resistors are not exceeded. Use extra resistors in series or parallel in place of a single resistor if it is predicted to dissipate more than 0.25 W.
6. If possible, the final selection of resistor values for each bias network must be based on a deterministic process and not trial and error. (This might not be possible for all of the resistors in the circuit in Figure 1b. In that case, limited use of trial-and-error is allowable.)
7. You may use Multisim or other circuit analysis software to check your design before you assemble the actual circuit. However, remember that the final design must be based on a deterministic process and not trial-and-error. Also remember that the MOSFET parameters k_n, V_t, and λ in the software model most likely will not match those of the physical MOSFET that you will use.
8. Keep careful records of your bias design process and test procedure since you will need to explain and justify them during your post-lab meetings.

- After you have completed your design, assemble the circuit around a 2N7000 MOSFET. Measure the quiescent drain voltage V_D, and determine the quiescent drain current I_D indirectly from your voltage measurements. Direct measurement of the current using the multimeter is too time-consuming. Confirm that both measured values are close to the specified values. You must determine whether the values are "close enough."

- Using a second 2N7000 MOSFET, design and assemble a three-resistor bias circuit (as in Figure 1b) to meet the same specifications as those for the four-resistor bias circuit. The second circuit should be assembled next to the first one. The value of R_D must be found deterministically, but you may use trial-and-error to find values for R_A and R_B. Adjust their values until the drain voltage is within 10% or so of its specified value. You may replace one or both resistors with a potentiometer to facilitate the adjustment. If you do, measure the resistance that the potentiometer adds to the circuit, and record the value.

- Perform a qualitative test of the stability of both bias circuits by warming each MOSFET using a hair dryer. Monitor the value of V_D, and continue applying heat until V_D stabilizes at a new value. Discuss the implications of the test with your group members and make sure that everyone understands what is happening. In particular, note whether the drain voltage rises or falls with temperature, and be able to explain the results in light of Figure 5 of the 2N7000 datasheet. Also read Section 5.4.4 of the textbook (Sedra & Smith, 8th ed.) for further information. (The section is very short.) Think about how the temperature variation of V_t compares to that of k_n and the degree to which each quantity might affect the value of I_D for the case when v_{GS} is barely greater than V_t and for the case when v_{GS} is much greater than V_t. That is, try to determine which effect dominates. In the saturation region,

$$I_D = \frac{1}{2} k_n \left(V_{GS} - V_t \right)^2 .$$

  Demonstrate the thermal test to the instructor before moving on to the next item **(In-lab Demo)**.

- Now add a function generator, three capacitors, and a load to the four-resistor bias circuit to form the common-source amplifier circuit shown in Figure 2. Component values and descriptions are listed below:

  - Input capacitor (C_i) with a value of 1.0 μF with the positive end connected to the gate terminal of the MOSFET.
  - Output capacitor (C_o) with a value of 1.0 μF with the positive end connected to the drain terminal of the MOSFET.
  - Source resistor bypass capacitor (C_S) with a value of 22 μF with the positive end connected to the source terminal of the MOSFET.
  - Load resistance (R_L) with a value of 100 kΩ connected to the negative end of C_o.
  - Function generator represented by the Thévenin equivalent circuit v_{sig} and R_{sig} connected to the negative end of C_i. Its frequency should be set to 1.0 kHz and its amplitude to 5 mV pk (Thévenin equiv. voltage) if possible. Some function generators have a minimum setting of 20 mV pp, so a 20 dB attenuator might be needed to reduce the input voltage to the amplifier to a sufficiently low level. A 20 dB attenuator reduces an applied voltage by a factor of 0.1 (why?) while maintaining a specified Thévenin equivalent output resistance (in this case, 50 Ω).
  - Oscilloscope with channel A connected across the output of the function generator and channel B connected across the load.

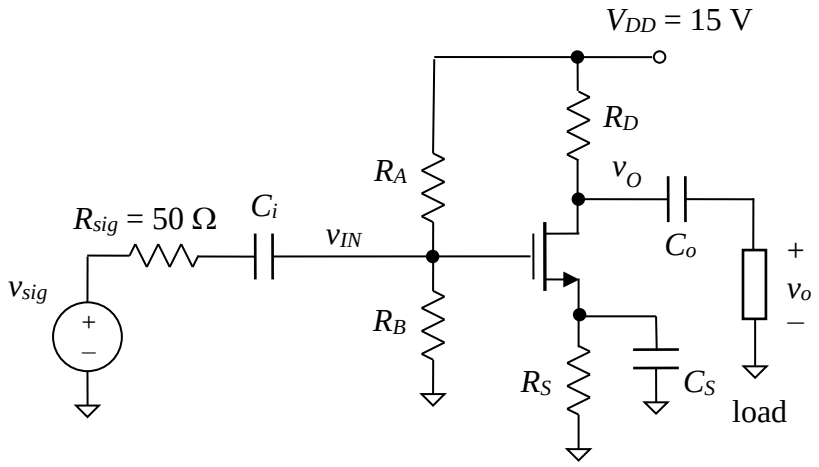

Figure 2. A basic common-source amplifier circuit.

- After the amplifier circuit has been assembled, apply power, and observe the input and output waveforms displayed on the oscilloscope. Adjust the oscilloscope's settings so that both waveforms are not too compressed in time and amplitude (i.e., so that the shapes of the two waveforms can be clearly seen). Make sure that neither the input nor the output waveform is experiencing distortion; they should be almost perfect sinusoids with no clipping and little to no flattening. The waveforms should be nearly symmetrical above and below the zero-volt level; if not, then some distortion is likely occurring, probably nonlinearity cause by the input voltage being too large. Use the measured amplitudes to calculate the voltage gain v_o/v_{in} of the amplifier, where v_o and v_{in} are signal voltages, not total voltages. Record this value for the post-lab meeting.

  Remember that the value displayed on the function generator display is half of the value of the actual Thévenin equivalent voltage v_{sig}.

- Using the measured bias voltages and/or currents obtained from your measurements and the known component values, calculate the value of the voltage gain using small-signal analysis. Initially assume that V_t = 2.1 V and k_n = 200 mA/V^2 as you did for the bias design step above, but then repeat your calculations by assuming that V_t = 2.0 V and k_n = 100 mA/V^2. Which set of assumptions yields better agreement with your measured gain value? Save both sets of calculations in a legible format for discussion during the post-lab meeting.

- Finally, increase the amplitude of the input voltage while monitoring the output waveform. Make sure that the details of the output waveform's shape are easy to see. At some point, you should begin to observe noticeable distortion from the expected sinusoidal shape. Increase the input voltage amplitude enough to cause significant distortion of the positive and negative peaks of the output waveform. Be prepared to explain the most obvious distortion effects and their causes during your post-lab meeting. Make sure that you can properly associate the region of operation of the MOSFET with each waveform feature (i.e., positive clipping, negative clipping, and portions without distortion).

- When you are confident that the amplifier is working properly and that you understand its behavior, schedule a post-lab meeting with me at a mutually agreed time before the deadline posted on the Laboratory page at the course web site. The following guidelines apply:

    - Read these guidelines, the following black bullet point, and the "Post-Lab Meeting" section below **well in advance of the meeting.** There are some changes from previous practices.
    - All group members must be present.
    - The meeting will take place in the Maker-E if Dana 307 is not available at the scheduled time.
    - Meetings will be scheduled in the order that requests are received. The order might be determined by random assignment.
    - Meetings will not be rescheduled if the first one reveals circuit problems, wiring failures, errors in the test procedure, or a lack of preparation.
    - Deadline extensions will generally be approved for confirmed illnesses or other extenuating circumstances.

- The visual aids that your group intends to use must be combined into a single PDF document and **e-mailed** to me before the post-lab meeting begins. Use a file name of the form:

    "LName1_LName2_LName3_Lab4_fa23.pdf"

    Add "LName4" if your group has four members. **The file size must be less than 5 MB.** Keep a copy of your documentation if you wish to use it to prepare for the next exam or need it for future reference.

<u>Post-Lab Meeting</u>

At the beginning of the post-lab meeting, your group must show that the amplifier is operating properly in general. The output waveform must have a substantially larger amplitude than the input waveform, and the output waveform must not be significantly distorted if the input signal is at a sufficiently low level. The oscilloscope must be adjusted so that both waveforms are clearly visible and easy to measure.

Each group member will then be asked to respond to one of the numbered prompts listed on the next page and possibly answer a few follow-up questions. Note the following:

- Your group may decide how the prompts are assigned. Each group member must answer a different prompt.
- Each person will have a time limit of **seven minutes** to respond.
- Responses must be supported by high-quality visual aids, including a properly labeled diagram (or diagrams).
- Organize the physical circuit layout so that group members can switch between demonstrations quickly.
- Excessive delays will affect the overall group score.

Special instructions regarding visual aids: In addition to the usual expectations of legible, well-organized, and readily accessible visual aids, any equations that you present **must** be prepared using software and conform to the guidelines given in "Formatting Guidelines for Equations and Technical Content," which is available on the Laboratory page at the course web site. If your favorite word-processing software does not have a good equation editor, consider using the CodeCogs Equation Editor, which is linked on the Laboratory page at the course web site. The quality, organization, and clarity of the visual aids will constitute a separate part of the overall lab score.

Individual prompts:

1. Explain the deterministic design process that your group followed for the four-resistor bias network. Justify any choices that were made to constrain the problem enough to obtain specific resistor values. Verify that the power limits for the resistors and the MOSFET were not exceeded.
2. Explain how the voltage gain of the amplifier was determined using small-signal analysis. The explanation should be supported by a small-signal model circuit diagram, a derivation of the voltage gain expression, and a calculation of the parameter g_m. Compare the calculated gain to the measured gain.
3. Explain the two most obvious impacts on the output waveform when the input amplitude is large enough to cause significant distortion. Explain why flattening of the positive and negative waveform peaks occurs and in what region (cut-off, saturation, or triode) the MOSFET operates in each case. Relate the observed distortion to the voltage transfer characteristic of the common-source amplifier (Figure 7.4b in Sedra & Smith, 8th ed.).
4. [Four-person group only:] Demonstrate how the voltage gain of the amplifier is determined using oscilloscope measurements. Include an explanation of how distortion is handled or minimized, whether peak or peak-to-peak measurements are used (and whether one or the other yields better results and why), whether the function generator imposes any limitations, and how noise on the waveforms is handled. Compare the measured gain to the calculated gain.

This portion of your lab score will be based on the clarity and accuracy of your responses, your understanding of the circuit's design and operation, and the quality of your visual aids. The latter must include a well-organized presentation of results and legible circuit diagrams with clearly labeled component values. It will be challenging to achieve a perfect score.

Lab Scoring Criteria

Each group member will receive a score based on the following criteria quantized at the indicated point values. The first two criteria constitute a group base score; that is, each group member will receive the same score for those two criteria. The remaining criteria will be assessed independently, and the corresponding scores will be determined by that person's contribution to the post-lab meeting. The rubrics posted on the Laboratory page at the course web site will guide the determination of the various scores.

0, 8, 15, 23, 30 pts	Functional bias circuits with completion of in-lab demo (group)
0, 8, 15, 23, 30 pts	Functional common-source amplifier (group)
0, 8, 15, 23, 30 pts	Quality of response to prompt (indiv.)
0, 2, 5, 8, 10 pts	Quality and effectiveness of supporting visual aids (indiv.)

If the meeting is completed after the deadline, a 10% score deduction will be applied for every 24 hours or portion thereof that it is late (not including weekend days) unless extenuating circumstance apply. No credit for the two individual criteria will be given four or more days after the deadline; however, up to 60 pts will be assigned to each member of the group for the first two (group) criteria if at least one group member demonstrates a functional circuit within a week of the deadline.

Group Assignments

The randomly generated groups for this lab exercise are listed below:

Beaudette-Beebe-Powick
Hackett-Jiorle-Regec
Flynn-Piper-Samuels
Bailey-Sagoe-Zhang
Andrews-Ren-Youn
Baganski-Jeong-Tuncel
Ashnault-Freedenberg-Miller