

Lab #4: Basic DC Power Supply
(Documentation requirements and scoring criteria revised 10/27/16)

Introduction

Because many types of electronic circuits are designed to be powered by DC sources, power supplies (sometimes called AC-to-DC converters) are found in most equipment that operates from commercial power outlets. At a minimum, a transformer, a rectifier circuit, and a filter capacitor are used to convert the AC voltage to a nearly constant DC voltage. In practice, sophisticated voltage regulation circuits are added to maintain the DC output voltage(s) at specified levels; however, the simple circuits that you will study in this two-week lab exercise form the foundation of most commercial DC power supplies. In fact, these basic circuits, with a few minor modifications, are sufficient for many applications in which a small amount of power supply “ripple” (noise) can be tolerated. An example is providing power to an array of light-emitting diodes (LEDs). Group assignments are listed at the end of this handout.

Theoretical Background

A very basic power supply circuit is shown in Figure 1. A source of AC, typically 120 V rms and represented here by v_{in} , drives a transformer that might step up or step down the voltage. The transformer’s secondary voltage, represented by v_{sec} in Figure 1, is therefore AC as well. If no load is present (i.e., the load is an open circuit), the capacitor charges during the first half-cycle that the diode is forward biased, that is, during the portion of the first positive half-cycle of v_{sec} for which $v_{sec} > V_F$, where V_F is the turn-on voltage of the diode. The capacitor voltage (v_o in Figure 1) during this time essentially equals v_{sec} minus the voltage drop across the diode because the internal resistance R_{sec} of the secondary winding and the diode resistance r_d are negligibly small, and the time constant $\tau = (R_{sec} + r_d)C$ that governs the capacitor charging rate is much less than the period of the sinusoidal voltage waveform. If a load is present and has an equivalent resistance R_L , then the time constant is given by $\tau = [R_L || (R_{sec} + r_d)]C$. (Do you know why?)

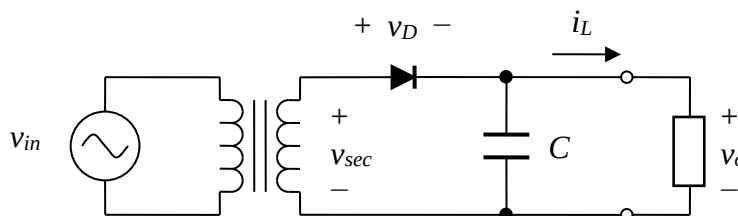


Figure 1. Basic power supply circuit using half-wave rectifier.

Of course, a load must be connected to the circuit if it is to serve any useful purpose. As shown in Figure 2, the output voltage v_o is not constant because the capacitor discharges though the load whenever v_{sec} falls below the level necessary to keep the diode forward-biased. Applying KVL to the circuit in Figure 1,

$$v_{sec} \approx v_D + v_o \rightarrow v_D \approx v_{sec} - v_o.$$

The approximation is due to the fact that there are small voltage drops across R_{sec} and r_d . Recall that the diode only conducts if $v_D = V_F$ can be maintained. As indicated by the KVL equation above, that condition is met only if $v_{sec} - v_o > V_F$. (The inequality is possible because of the small voltage drops across R_{sec} and r_d .) Since v_o stays fairly close to the peak positive value of v_{sec} (minus V_F) at all times because of the slow discharge of the capacitor, the diode conducts during only a short portion of the positive half-cycle of v_{sec} . (The positive half-cycle is near its peak only briefly.) During the negative half-cycles of v_{sec} , the diode is reverse biased because $v_{sec} - v_o$ is negative. Thus, the voltage across the capacitor remains close to the peak positive value of v_{sec} minus the value of the diode's turn-on voltage if the capacitor's value is large enough.

This circuit is called a *half-wave rectifier* because it allows current to flow in only one direction through the load ("rectifier") and because current flows through the diode during part of only one of the two half-cycles ("half-wave"). Although the load current i_L is unidirectional and therefore technically DC, its value fluctuates as the capacitor voltage rises and falls.

The fact that the diode conducts during only one of the AC voltage's half-cycles is a major disadvantage of the half-wave rectifier circuit. As shown in Figure 2, during the half-cycle when the diode does not conduct the capacitor continues to discharge through the load. During this time the capacitor and load are effectively isolated from the rest of the power supply circuit, and the capacitor voltage drops exponentially with the time constant $R_L C$. If R_L is relatively small, the current flowing out of the capacitor when the diode is off will be significant, and the voltage across the capacitor could drop to an intolerably low level. The smaller the value of R_L , the smaller the time constant, and therefore the more quickly the capacitor discharges. The only way to remedy this situation is to increase the size of the capacitor. However, large capacitors are expensive, bulky, and heavy compared to other components.

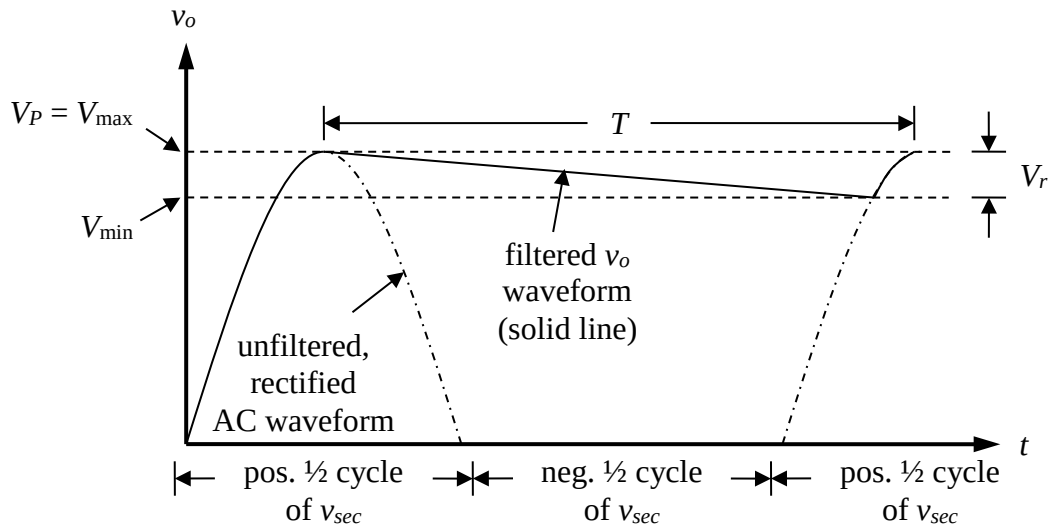


Figure 2. Depiction of ripple on the output voltage waveform of a DC power supply with a filtered half-wave rectifier. The period T is the reciprocal of the AC frequency f . The peak output voltage V_P is equal to the peak secondary voltage minus one diode drop V_F .

The alternating charge and discharge cycles cause the output voltage of the power supply to fluctuate between a minimum value $V_{\min}$ and a maximum value $V_{\max}$, resulting in what is called a *ripple voltage* V_r that is superimposed on the average DC output voltage. Since most loads require a nearly steady supply of DC, the presence of a significant ripple voltage is undesirable. The ripple voltage is sometimes expressed as a percentage and is calculated using the formula [1]

$$\% \text{ ripple} = 100 \frac{\text{peak - to - peak ripple voltage}}{\text{average DC voltage}}.$$

Since the average voltage might not be easy to predict, the percentage ripple is often approximated using

$$\% \text{ ripple} \approx 100 \frac{\text{peak - to - peak ripple voltage}}{\text{peak DC voltage}} = 100 \frac{V_r}{V_p}.$$

The capacitor shown in Figure 1 is called a *filter capacitor* because its purpose is to reduce the ripple voltage to an acceptable level.

The presence of ripple in the output of a power supply can be mitigated partly by using a *full-wave rectifier* circuit like the one shown in Figure 3. In this circuit, diodes D_2 and D_4 conduct during part of the positive half-cycles of v_{sec} , and diodes D_1 and D_3 conduct during part of the negative half-cycles. During both half-cycles current flows downward through the load. As with the half-wave rectifier, the diodes conduct for only a small part of each half-cycle because the slowly falling voltage v_o across the filter capacitor C ensures that the diodes are off ($v_D < V_F$) most of the time.

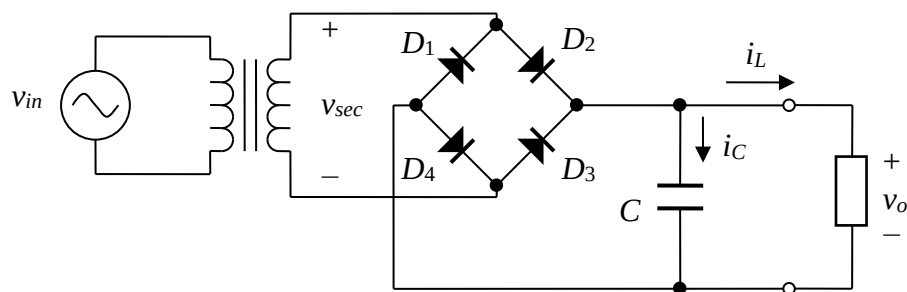


Figure 3. Full-wave bridge rectifier circuit with filter capacitor.

As shown in Figure 4, the full-wave rectifier is an improvement over the half-wave circuit because the capacitor charges during part of both half-cycles. Consequently, the capacitor does not have as much time to discharge, and the output voltage does not drop as far. For a given target ripple voltage only about half the filter capacitance is needed relative to that required in the half-wave rectifier. The only disadvantages of the full-wave circuit are the increased cost, weight, and space required for four diodes (this usually turns out not to be significant) and the larger $2V_F$ voltage drop between the secondary voltage peak and the load voltage v_o .

It should be clear by now that the selection of an appropriate value for the filter capacitor is an important design consideration. Fortunately, the value of C required for a given ripple voltage

specification is easily determined. The current i_c that flows into the upper end of the filter capacitor in Figure 3 is related to the capacitor's voltage (which is equal to v_o) by

$$i_c = C \frac{dv_o}{dt}.$$

If the ripple is a small percentage of the total output voltage, then the voltage across the capacitor decays almost linearly, as shown in Figure 4. Voltage $V_{\max}$ is the maximum value of the output voltage, and $V_{\min}$ is the minimum value. If the ripple is small, then the capacitor will not start charging again until almost the next time the secondary voltage reaches its peak value (represented by $|v_{\text{sec}}|_{\text{pk}}$). For a full-wave rectifier, the next voltage peak occurs one half-period ($0.5T$, where T is the period) later. The time derivative of the output voltage can therefore be approximated as

$$\frac{dv_o}{dt} \approx -\frac{V_{\max} - V_{\min}}{0.5T},$$

where the negative sign indicates that the output voltage falls as the capacitor discharges (negative slope). Substituting this result into the i - v relationship for the capacitor yields

$$i_c = C \frac{dv_o}{dt} \approx -C \frac{V_{\max} - V_{\min}}{0.5T}.$$

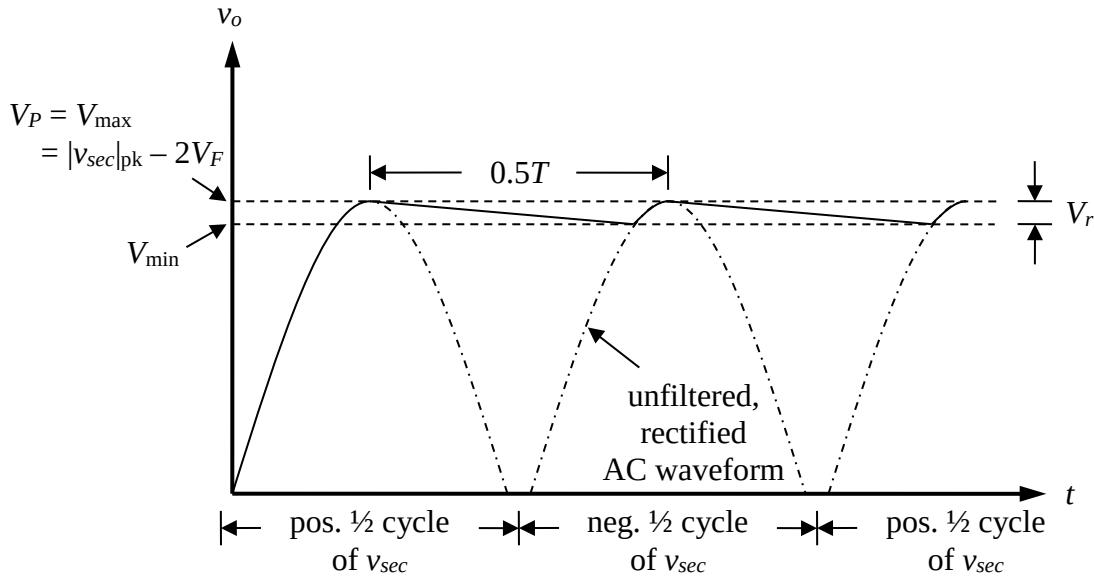


Figure 4. Ripple in the output voltage waveform of a DC power supply with a full-wave rectifier. The period T is the reciprocal of the AC frequency f . The filter capacitor discharges for only half a period before it is recharged to the peak voltage V_P . The output voltage therefore drops only half as far as that in a half-wave rectifier for the same C value and load. The peak voltage V_P is equal to the peak secondary voltage magnitude minus two diode drops ($2V_F$).

The diodes are off when the capacitor discharges, so the only place the capacitor current can flow is through the load. Since i_c is defined as flowing into the upper end of the capacitor, this means that $i_c = -i_L$ when the capacitor discharges, and

$$i_L = -i_c \approx C \frac{V_{\max} - V_{\min}}{0.5T}.$$

The ripple voltage V_r is defined as the extent of the fluctuation of the output voltage, so $V_r = V_{\max} - V_{\min}$. Thus,

$$i_L \approx C \frac{V_r}{0.5T}.$$

Multiplying the numerator and denominator of the right-hand side by V_P and using the relationship $T = 1/f$, where f is the frequency of the AC waveform, lead to

$$i_L \approx C \frac{V_r}{0.5T} \frac{V_P}{V_P} = \frac{2C(V_r/V_P)V_P}{T} = 2fC(V_r/V_P)V_P.$$

The quantity in parentheses is the “fractional” ripple, that is, the ripple amplitude expressed as a fraction of the peak output voltage. For example, if the percentage ripple is 5%, then the fractional ripple is 0.05 (unitless). The fractional or percentage ripple is an important power supply specification, and in the simple circuit discussed here it is related to the filter capacitor size and the load current magnitude.

In a typical power supply application, a specific voltage must be supplied to the load, and the current demanded by the load will vary over some range. The largest expected load current $i_{L\max}$ will be associated with the fastest discharge of the capacitor during each half-cycle and therefore the largest ripple. Thus, the minimum required filter capacitance to meet a given ripple specification at maximum load current can be found by solving the equation above for C and assigning the maximum possible value to i_L . The result is

$$C_{\min} = \frac{i_{L\max}}{2f(V_r/V_P)V_P}.$$

Recall that voltage V_P is the nominal DC output voltage of the power supply.

The output voltage of the simple DC power supply discussed here is approximately two diode voltage drops (roughly 2.0 V) below the peak magnitude of the secondary voltage ($|v_{\text{sec}}|_{\text{pk}}$). If a particular output voltage level is required for a given application, then a transformer must be selected that has the appropriate peak secondary voltage rating. This can be a significant limitation, since not many secondary voltage options are available. In a later lab exercise we will study one method for obtaining almost any desired output voltage level that lies below the secondary voltage peak. The particular value of the secondary voltage is not critical in that case.

Reference

1. M. Wasserman, *Laboratory Manual for Microelectronic Circuits and Devices*, 2nd ed., by M. N. Horenstein, Prentice-Hall, Inc., Upper Saddle River, NJ, 1996.

Experimental Procedure

STOP! Before proceeding, please read and understand the following two very important warnings. If they are not clear to you, please discuss them with the instructor or TA.

Warning #1: Do not attempt to measure both the AC voltage on the secondary winding of the transformer (v_{sec}) and the output voltage across the load (v_o) with the oscilloscope at the same time. If you try to do this, the ground leads will create a short across diode D_4 in Figure 3 that will most likely lead to the destruction of diode D_1 . You should trace the circuit connections in Figure 3 and understand how this can happen before proceeding.

Warning #2: Electrolytic capacitors are polarized. Failure to pay attention to their polarity could result in their spectacular destruction, an unpleasant smell for everyone nearby, and possible personal injury. The marking on an electrolytic capacitor's package usually indicates its *negative* terminal (i.e., a negative sign is printed on the package).

- Design and assemble a DC power supply with a full-wave bridge rectifier like the one shown in Figure 5. This circuit is identical to the one shown in Figure 3, except that a load consisting of three LEDs wired in parallel has been added. A transformer will be supplied to you. For safety reasons, the transformer is enclosed in a box with a power cord and a circuit breaker. As shown in Figure 6, there are three jacks on the box that are connected to the secondary winding. The two red jacks connect to the ends of the secondary winding, and the green jack connects to a center tap. For this lab experiment, take the AC voltage for your power supply between the green jack and one red jack. Before you can design your circuit, you will need to determine the secondary voltage of the transformer by measurement. Be aware that the waveform might not be perfectly sinusoidal. Power line noise caused by computer power supplies and heavy equipment in the vicinity lead to the presence of significant harmonics in the local line voltage.

The power supply should have the following specifications:

Diode type: 1N4001 or 1N4007 (data sheet available on lab page)

Peak DC output voltage: whatever is available from the transformer, minus two diode drops

Max. expected load current: enough to produce a relative luminous intensity of 1.0 from each LED (data sheet available on lab page)

Max. percentage ripple: 5%

You might need to use a value for the filter capacitor that exceeds any single value available in the parts bins. You may combine capacitors in series and/or parallel to achieve the desired capacitance, but use good design practice and avoid overdoing it. Keep in mind that the

tolerance of electrolytic capacitors is typically 20-40% and that electrolytic capacitors are bulky and relatively expensive. Your filter capacitor network (and its complexity) should be consistent with that tolerance range. A design that uses an excessive number of capacitors in an effort to achieve an exact value will be viewed unfavorably!

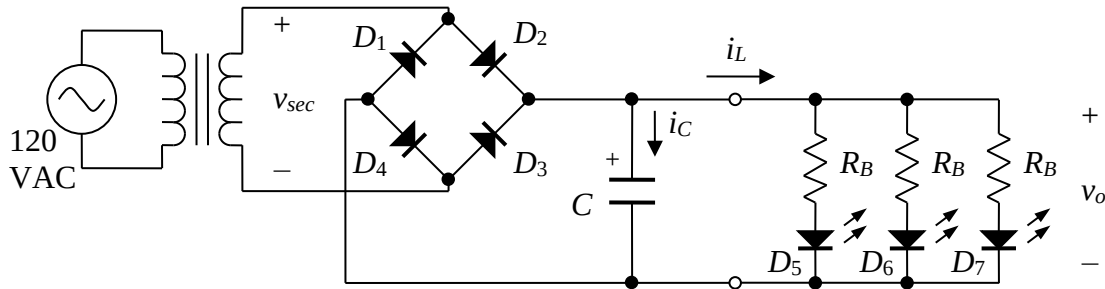


Figure 5. Full-wave bridge rectifier circuit with filter capacitor and three-LED load. The LED current-limiting resistors R_B all have the same value. The “+” symbol next to the upper plate of the capacitor indicates that it is an electrolytic type. Electrolytic capacitors are commonly used in power supply circuits because they are available in large values.

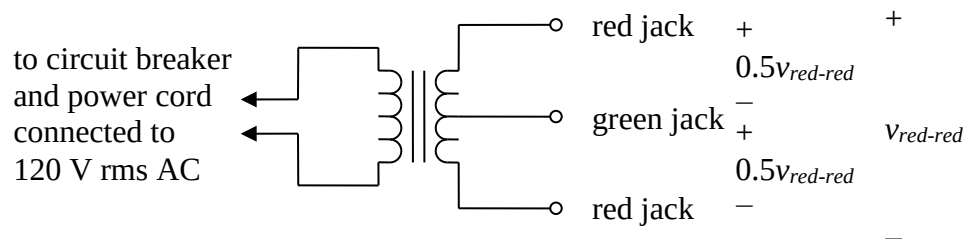


Figure 6. Connections to transformer inside its enclosure.

- **Before applying power**, check the power dissipation levels of all resistors and ensure that they are being used within their ratings. If any are not, redesign your circuit. Use a $2\times$ safety factor.
- Display the output voltage waveform on the oscilloscope, and check whether or not your power supply meets the specifications. Troubleshoot any problems.
- Once you are confident that the power supply is working properly, demonstrate it to the instructor. A complete demonstration includes discussing your capacitor network design and verifying that none of the resistors' or other components' power ratings are being exceeded. Show the output voltage waveform for the specified three-LED load with and without the filter capacitor in place.

Note: The ripple voltage might be so low that you will have to adjust the oscilloscope's trigger controls to stabilize the displayed waveform. If that does not work, then you might

have to switch to a more sensitive vertical scale and move the 0-V level off the screen. You can determine the peak output voltage and ripple voltage using the manual cursors. Also remember to use the “BW Limit” feature to minimize the noise from WVBU.

Lab Documentation [revised 10/26/16]

After the lab sessions are over, compile the following items into a single electronic document:

- a. A brief introductory section that focuses the reader’s attention from a broad overview or perspective to the specific topic(s) under discussion.
- b. Report the actual filter capacitance used in your circuit, and use the screen capture (with appropriate annotations and caption) of the output voltage waveform that you obtained to verify that the ripple voltage corresponds correctly to the load current drawn by the three LEDs. That is, explain whether or not the relationship

$$i_c = C \frac{dv_o}{dt}$$

is approximately true for your circuit during the capacitor discharge intervals. Explain all of the approximations that you use, where all of the values you use come from, and under what conditions the behavior you are describing applies. You should also discuss the extent to which the specifications were (or were not) met or exceeded, and why. Discuss any limitations to the inferences you can draw because of noise on the waveform or other non-ideal factors.

- c. A brief concluding section that brings about a satisfying sense of closure for the reader. It should include a brief interpretation of your results and observations and/or a discussion of implications. Your ideas should be at least partly original. Do not simply repeat information that has already been given in the course except to elaborate on them in new ways. Highlight outcomes, ideas, relationships, impacts, implications, issues of concern, and so forth that the reader might miss without your guidance, but avoid rambling, vague, and/or excessively far-reaching statements. This section should be a brief but thoughtful reflection on your results and what they would mean to a manager or supervisor.

The documentation must be in MS-Word (*.doc or *.docx) format using 11-point or larger font. Multiple text columns per page may not be used. The total length of the text must not exceed 900 words, but any number of supporting figures, tables, equations, and/or other graphics may be added. Include the group members’ names, the course number (ECEG 350), the lab session dates (Sept. 29-Oct. 6), and the lab number on the first page. A cover sheet is not required. Use the file naming convention described at the lab web site. One copy per group must be submitted via the course Moodle site by **11:59 pm on Thursday, November 3 [new date]**.

The documentation should be thorough, well organized, clear, legible, concise, and professional in tone and style. It must also exhibit good writing mechanics, spelling, and grammar. Equations must be type-set using one of the equation editors available in MS-Word. Figures may be neatly hand-drawn, scanned or photographed, and inserted into the document. Minimize the file size by using appropriate camera or scanner settings (e.g., black & white and 300 dpi for scanning). All four margins (top, bottom, left, right) should be at least one inch. Single line spacing is acceptable. Keep a copy of your documentation if you wish to use it to prepare for the next

exam. Pay close attention to the issues addressed in the “Lab Documentation Guidelines” available at the lab web site.

Lab Scores [revised 10/26/16]

Each group member will receive the same overall score according to the following criteria. Scores will be quantized at the indicated percentage levels following the rubric posted at the lab web site:

0, 20, 40, 60, 70%	Demonstration of basic power supply with filter capacitor
0, 2, 5, 8, 10%	Items listed in the “Lab Documentation” section

If the demonstration is completed after the deadline, a 10% score deduction for every 24 hours or portion thereof that it is late will be applied (not including weekend days). No demonstration credit will be given four days or more after the deadline.

Lab documentation submitted after the deadline will have a 10% score deduction applied for every 24 hours or portion thereof that it is late (not including weekend days), although credit for a successful demonstration (60% maximum) will be recorded regardless of when the documentation is submitted.

Group Assignments

The randomly generated groups for this lab exercise are listed below:

1 pm section

Natalie-Muller

Taylor-Liu

Pencak-Harrington

Chambers-Ouellette

Scott-Huang

Morlock-Malmquist

Kumaran-Lenk-Panzarino

3 pm section

Szybist-Woodford

Poulton-Greenberg

Bilcheck-Haberle

Xu-Prajapati

Farrell-Rumachik

DiDomenico-Glickman

Petrimoulx-Ye

Chen-Sabah

Kyaw-Mendelowitz

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