Lab #5: CMOS Logic Gates

Introduction

Digital circuitry forms the foundation of the modern technical, information-centric world. All digital circuits, from simple combinational logic circuits to sophisticated microprocessors, employ logic gates that perform the basic Boolean functions such as AND, OR, NAND, NOR, etc. All of the basic logic gates are implemented in the major logic families. The CMOS (complementary metal-oxide semiconductor) family is currently the most widely used because of its low power dissipation properties, its relatively low cost of fabrication, and its high density of gates in integrated circuit (IC) chips. In this lab exercise you will analyze the operation of a basic CMOS logic gate. Group assignments are listed at the end of this handout.

Theoretical Background

The fundamental logic gate in any logic family is the NOT gate, or inverter. The output of a NOT gate is the complement of the input. That is, a logical input of 0 yields a logical output of 1, and vice versa. The other fundamental types of combinational logic gates, the AND, OR, NAND, NOR, XOR, and XNOR gates, have two or more inputs. For two-input gates with inputs labeled A and B, the following truth table defines the output states for the indicated Boolean operations.

Inputs		Boolean Operation					
A	*B*	AND	NAND	OR	NOR	XOR	XNOR
0	0	0	1	0	1	0	1
0	1	0	1	1	0	1	0
1	0	0	1	1	0	1	0
1	1	1	0	1	0	0	1

In the CMOS logic family, these Boolean operations are implemented on IC chips that contain both p-channel (PMOS) and n-channel (NMOS) MOSFETs. For enhancement-mode NMOS devices in normal operation, the drain current i_{Dn}, the gate-to-source voltage v_{GSn}, the drain-to-source voltage v_{DSn}, the threshold voltage V_{tn}, and the transconductance parameter $k_n = \mu_n C_{ox} W/L$ are all positive quantities. For PMOS devices, the quantities i_{Dp}, v_{SGp}, v_{SDp}, and the parameter $k_p = \mu_p C_{ox} W/L$ are also positive, but the threshold voltage V_{tp} is negative. Positive drain current is defined as flowing out of the drain terminal in PMOS devices.

Typical i-v characteristics for NMOS and PMOS devices are shown in Figure 1. During normal operation, all NMOS devices in the equilibrium state, which is defined as the case when the input and output voltages have settled to either a logical 0 or 1 representation, have gate-to-source voltages of either 0 V or V_{DD}, and all PMOS devices have source-to-gate voltages of either 0 V or V_{DD}. This implies that the operating point of each device lies along either the upper curve in one of the plots in Figure 1 or along the horizontal axis, which corresponds to the cut-off region. Note that the v_{GSn} or $v_{SGp} = V_{DD}$ curves and the v_{GSn} or $v_{SGp} = 0$ "curve" (the horizontal axis) in each plot intersect at the origin.

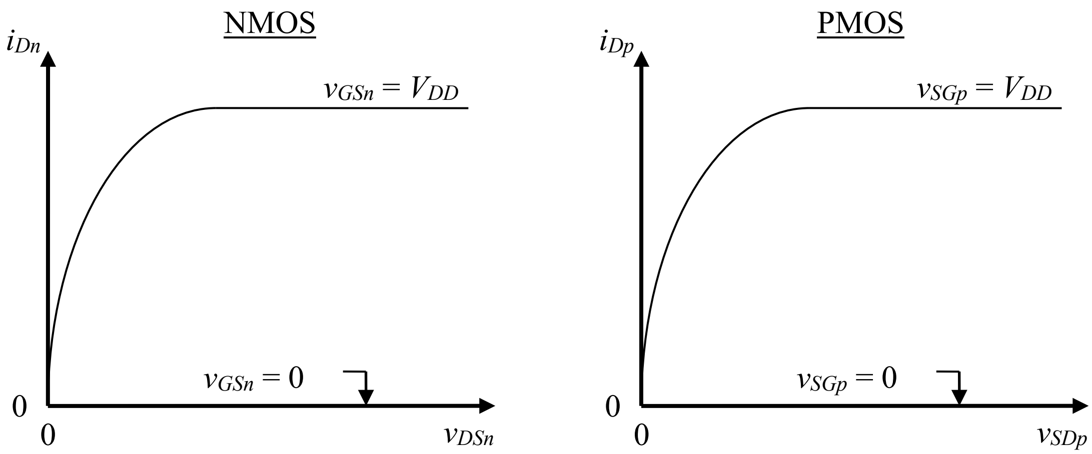

Figure 1. Graphical representations of the *i*-*v* characteristics for *n*-channel (left) and *p*-channel (right) MOSFETs for two different values of the gate-to-source or source-to-gate voltage. These represent the two possible equilibrium states of a MOSFET in a CMOS logic gate (i.e., not transitioning between logical states).

When in the equilibrium state, the transistors in a CMOS logic gate operate in either the cut-off region or the triode region because the drain current through all of the transistors is practically zero. Examination of Figure 1 shows that an NMOS device or a PMOS device can have zero drain current when it is in the triode region if v_{DSn} or $v_{SDp} = 0$. The region of operation is determined by the value of v_{GSn} for NMOS devices and by v_{SGp} for PMOS devices.

Experimental Procedure

You will be given a blank truth table and a circuit diagram for a CMOS logic gate that implements an unknown (to you) Boolean operation. The NMOS and PMOS symbols used in the diagram have the more complicated form that includes the substrate (body) terminal. The reason for this will be explained at the beginning of the lab session. Complete the following items:

- Using the NMOS and PMOS *i*-*v* characteristics in Figure 1 as a guide, complete the truth table for the circuit, and determine the Boolean operation (NOT, AND, OR, NAND, NOR, XOR, or XNOR) that the circuit implements. Also determine the region of operation of each of the four MOSFETs for each input state (00, 01, 10, and 11). Add all of this information as well as your names to the Microsoft Word file corresponding to the gate type assigned to your group. Also indicate the logical gate type. The documents with the circuit diagrams and truth tables are available on the Laboratory page at the course web site.

  During your group's post-lab meeting, each group member will be required to explain how you determined the gate's logical output state and the regions of operation of all four MOSFETs for one of the input cases. Your explanation must be thorough and detailed, including how you determined the value of each relevant voltage and current in the circuit. The diagrams in Figure 1 should be an integral part of the explanation. You may not assume any voltage or current values without evidence. For example, you may not refer to the part of the Theoretical Background section that states that "the drain current through all of the transistors is practically zero" as a starting point; you must explain *why* the current is practically zero.

You will discover that determining the region of operation for one of the MOSFETs will be more challenging than for the other three, particularly for one of the four input states. For Gate A, it is Q_3 for input state $A = 1$, $B = 0$, and for Gate B, it is Q_2 for input state $A = 1$, $B = 0$. However, for that case you should be able to predict the overall output state of the logic gate regardless of the operating region of that particular MOSFET. The group member who is assigned input state $A = 1$, $B = 0$ will not be expected to determine the region of operation of the especially challenging MOSFET. However, if that person wants to take on the challenge, then they should start by assuming one of the two likely possibilities and then look for contradictions.

- After you have completed the truth and region-of-operation table and everyone in your group understands how the circuit operates, schedule a meeting with me to take place at a mutually available time before the end of the semester. Time slots will be available during the last lab sessions of the semester on Tuesday, December 9, or you may meet with me earlier if you wish. If your group completes your post-lab meeting before December 9, then you do not have to attend that lab session. The following guidelines and instructions apply:

    - All group members must be present, but you do not have to remain in the lab room after your group's meeting has ended.
    - Meetings will initially be randomly scheduled during the lab sessions on Tuesday, December 9, but, as explained above, you may request an earlier meeting.
    - Requests for early meetings (to take place before the lab sessions) will be handled in the order in which they are received. Meetings may not conflict with a lecture, lab, or recitation for another course or during important work, athletic, performance, or similar commitments. Please notify me of time conflicts.
    - Meetings will not be rescheduled if the first one reveals a lack of preparation.
    - If a confirmed illness or other extenuating circumstance prevents you from attending your group's post-lab meeting, then you will most likely have to make it up after you have completed your final exams. An earlier make-up meeting must be requested in writing or via e-mail. This policy is necessary because the lab sessions take place at the end of the last day of the semester.

- Before the meeting, e-mail to me the completed MS-Word worksheet corresponding to the logic gate type assigned to your group. Name the file "LName1_LName2_LName3_Lab5_fa25.docx," where LName1, etc. are the last names of your group members. Add a fourth last name if necessary.

Post-Lab Meeting

During the meeting, each lab group member must explain how the logical output state and the regions of operation of all four MOSFETs were determined for one of the logical input combinations listed below. Your explanation must be thorough and detailed, including how you determined the value of each relevant voltage and current in the circuit.

- $A = 0, B = 0$
- $A = 0, B = 1$
- $A = 1, B = 1$
- $A = 1, B = 0$ if the group has four members

The following guidelines and instructions apply to the post-lab meeting:

- Your group may pre-assign input states to individual members; that is, input states do not have to be randomly selected during the meeting.
- Each person will have a time limit of **six minutes** to complete their explanation. Due to the tight schedule, the time limit will be strictly enforced.
- Excessive delays will affect group and/or individual scores as appropriate.
- If the group has only three members, then there will be a general discussion regarding the $A = 1, B = 0$ input state (the fourth one listed above).
- Each explanation must be supported by high-quality visual aids prepared by the respondent, including a properly labeled circuit diagram. Ideally, a separate diagram should be prepared by each group member to support their specific explanation. Consider including additional graphics to further support your explanation. **All tables, equations, variables, and other mathematical content must be formatted according to the guidelines** posted on the Laboratory page at the course web site. If your word-processing app does not have a good equation editor, consider using the CodeCogs Equation Editor, which is linked on the Laboratory web page. **Data tables, if used, must be prepared using software.** Graphics such as circuit diagrams may be prepared by hand, but they must be very neat and legible.
- Visual aids must be complete enough for understanding but not so information-packed that they are overwhelming or create visual clutter that detracts from clarity.
- Individual scores will be based on the accuracy and thoroughness of the response, the comprehension of the applicable concepts, and overall preparation for the meeting.

Extra Credit Opportunity

Your group may complete **one** of the following two options to add up to 10 points to each group member's overall score. Each member who wishes to receive extra points must be present at the demonstration. The demonstration must be completed within **five minutes**; no extensions will be granted for wiring or software issues. If there is time, the demonstrate may take place at the end of the post-lab meeting; otherwise, you may schedule a separate in-person or Zoom session with me. No assistance will be provided by me for either option. Presentation quality and circuit operation will carry equal weight. The number of points added will be determined as follows:

10 pts – proper operation with clearly labeled terminals and clearly indicated input and output states/voltages; circuit operation must be clearly and efficiently presented
7 pts – minor deficiency in one or two of these requirements
5 pts – major deficiency in one or two of these requirements
2 pts – multiple deficiencies

- **Option 1:** Simulate the logic gate assigned to your group in *Multisim*. You must use *Multisim* voltage probes to monitor the gate's output voltage v_O and the node voltage between the two "stacked" MOSFETs (Q_3 and Q_4 in gate A and Q_1 and Q_2 in gate B). You must also use SPDT (single-pole, double-throw) switches at the input terminals to allow rapid, real-time changes of the input voltages from 0 V (logical 0) to V_{DD} (logical 1). Change the key designations of the switches to "A" and "B" to match the input labels. Use the generic MOS_N_4T and MOS_P_4T devices available in the "TRANSISTORS_VIRTUAL" family of the "Transistors" component group. You must provide appropriate connections between the substrate (body) terminal and either ground or V_{DD} for each MOSFET. This provides a realistic simulation of actual CMOS devices because the substrate terminals cannot always be shorted to the source terminals in integrated circuits.

- **Option 2:** Construct and demonstrate a physical version of the logic gate assigned to your group using the CD4007 chip available via the ECE Department's component database. (Look for "CMOS Dual Complimentary Pair" in the Misc. ICs section.) A datasheet for the CD4007 is available on the Laboratory page at the course web site. Design your layout so that the logic gate's output voltage v_O and the node voltage between the two "stacked" MOSFETs (Q_3 and Q_4 in gate A and Q_1 and Q_2 in gate B) can be easily measured using the benchtop multimeter. Devise an efficient way to switch each input terminal between logical 0 (0 V) and logical 1 (V_{DD}) to allow rapid, real-time changes. Clearly label or otherwise indicate input *A* and input *B*.

Lab Scoring Criteria

Each group member will receive a score based on the following criteria quantized at the indicated point values. The first criterion constitutes a group base score; that is, each group member will receive the same score for that criterion. The remaining criteria will be assessed individually and will be determined by that person's contribution to the post-lab meeting. The rubrics posted on the Laboratory page at the course web site will guide the assignment of scores.

0, 20, 40, 50, 55, 60 pts	Properly completed truth and region-of-operation table (group)
0, 2, 5, 8, 10 pts	Quality and effectiveness of supporting visual aids (indiv.)
0, 8, 15, 23, 30 pts	Quality of response to prompt (indiv.)

According to university policy, meetings may not take place after classes end for the semester. Thus, partial credit for a late meeting will not be available. However, if the meeting is not completed, each member of the group can receive up to 60 pts (same score for each member) if the worksheet containing the completed truth and region-of-operation table is e-mailed to me by 11:59 pm on Tuesday, December 9.

Group Assignments

The randomly generated groups for this lab exercise are listed below. The letter next to your group indicates your assigned logic gate circuit.

1:00 pm Section:
Cherniske-Foster-Golden-Prevuznak (A)

3:00 pm Section:
Chernova-De La Cruz-Kraiker-Pan (B)
Charles-English-Rios Saldivar-Vaccaro (A)
Bui-Manicke-Ortiz-Wu (B)