ECEG 350L Electronics I Laboratory Fall 2023

**Lab #5: Logic Gate A**

Group Members: 1) Logical gate type:

 2)

 3)

The circuit shown below is a logic gate made entirely of enhancement-mode MOSFETs. The two upper transistors (*Q*1 and *Q*2) are PMOS devices, and the two lower ones (*Q*3 and *Q*4) are NMOS devices. Wires in the diagram that cross without a dot are not connected together. The MOSFET symbols below are an alternate form that includes the connection to the substrate. Note that the arrows point “backwards” relative to the arrows in the simpler symbols that we have been using.

The substrate of the upper NMOS transistor (*Q*3) is connected to ground instead of to its source terminal. This means that the source-to-substrate voltage (*vSB*) for that transistor could be non-zero. A non-zero value of *vSB* causes the value of the threshold voltage *Vt* for that transistor to be slightly higher in magnitude than the *Vt* values for the transistors that have their sources tied to their substrates (for which *vSB* = 0). In digital logic circuits the effects of a non-zero *vSB* are usually not significant since the applied gate-to-source voltages (0 V or ±*VDD*) are well above or below the altered *Vt* value in magnitude.

*Q*2

*Q*1

*Q*3

*Q*4

*vo*

*vA*

*vB*

*VDD*

|  |  |  |
| --- | --- | --- |
| Inputs | LogicalOutput | Region of Operation |
| *A* | *B* | *Q*1 | *Q*2 | *Q*3 | *Q*4 |
| 0 | 0 |  |  |  |  |  |
| 0 | 1 |  |  |  |  |  |
| 1 | 0 |  |  |  |  |  |
| 1 | 1 |  |  |  |  |  |

Choices: C = Cut-off, T = Triode, S = Saturation