ECEG 351 **Electronics II** **Spring 2024**

Policies and Review Topics for Exam #1

The following policies will be in effect for the exam. They will be included in a list of instructions and policies on the first page of the exam:

1. You will be allowed to use a non-wireless enabled calculator, such as a TI-89.
2. You will be allowed to use one 8.5 × 11-inch two-sided handwritten help sheet. No photocopied material or copied and pasted text or images are allowed. If there is a table or image from the textbook or some other source that you feel would be helpful during the exam and that is not included on the table and formula sheet that I will provide, please notify me.
3. All help sheets will be collected at the end of the exam but will be returned to you later.
4. **You may not leave the exam room without prior permission except in an emergency or for an urgent medical condition. Please use the restroom before the exam.**

The following is a list of topics that could appear in one form or another on the exam. Not all of these topics will be covered, and it is possible that an exam problem could cover a detail not specifically listed here. However, this list has been made as comprehensive as possible.

Although significant effort has been made to ensure that there are no errors in this review sheet, some might nevertheless appear. The textbook and the supplemental readings are the final authority in all factual matters, unless errors have been specifically identified there. You are ultimately responsible for obtaining accurate information when preparing for the exam.

Qualitative understanding of BJT operation

- *npn*: thin *p*-type base sandwiched between *n*-type emitter and collector
- *pnp*: opposite of *npn*
- base-emitter (B-E) and collector-base (C-B) junctions are regular *pn* junctions and have many similarities to *pn* junction diodes (i.e., they can be forward or reverse-biased; they have turn-on voltages)
- turn-on voltage (V_F) is approx. 0.7 V for Si; most BJTs are made from Si
- effect of changing base current i_B
- effect of changing collector-emitter voltage v_{CE} (normally C-B junction is reverse biased or at least not heavily forward biased; necessary for collector current to flow)
- directions and polarities of important currents and voltages (i_B, i_C, i_E, v_{BE}, v_{CE})
- thin base region allows electrons (*npn*) or holes (*pnp*) to flow from emitter to collector
- emitter more heavily doped than base – allows base to fill with minority charge carriers (electrons in *p*-type base for *npn*; holes in *n*-type base for *pnp*) when base current flows
- base-emitter junction is forward biased if v_{BE} (or v_{EB} for *pnp*) is at turn-on voltage (V_F)
- *i*-*v* characteristic of B-E junction is the same as that of a *pn*-junction diode:

  $i_B = I_{SB} e^{v_{BE}/\eta V_T}$,

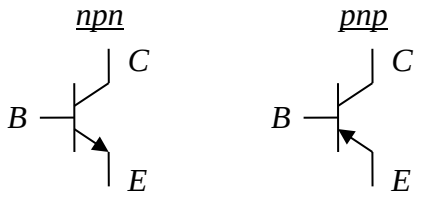
  where I_{SB} = saturation current of B-E junction, η = emission coefficient (typically assumed to equal one), and V_T = thermal voltage, which is given by

  $V_T = \dfrac{T}{11{,}600}$, where T = temperature in kelvins ($V_T \approx 25$ mV at room temp.)

- collector-base junction is usually reverse biased (produces depletion region) or lightly forward biased; in either case, the built-in E-field across the C-B junction is sufficiently strong to draw most of the minority carriers in the base into the collector
- collector current related to base current by $i_C = \beta i_B$ in the active region, where β = forward DC current gain (values are typically 20–300 for *npn*, but vary among BJT types, even among individual units of a given type within the same manufacturing batch)
- β varies strongly with temperature

BJT circuit symbols

- pay attention to directions of arrows (arrow indicates the emitter terminal and BJT type; arrow of *npn* is "*n*ot *p*ointing i*n*"; arrow indicates direction of emitter current)
- *pnp* symbol usually drawn "upside down" so that i_C and i_E flow downward



npn vs. *pnp* BJTs

- v_{BE} and v_{CE} of *npn* BJTs normally have positive values
- v_{BE} and v_{CE} of *pnp* BJTs normally have negative values (use v_{EB} and v_{EC} instead)
- i_B and i_C flow *into* base and collector terminals of *npn* BJTs and *out of* base and collector terminals of *pnp* BJTs; i_E flows *out of* emitter of *npn* and *into* emitter of *pnp*
- β varlue of *npn* BJTs is usually much larger than that of *pnp* BJTs

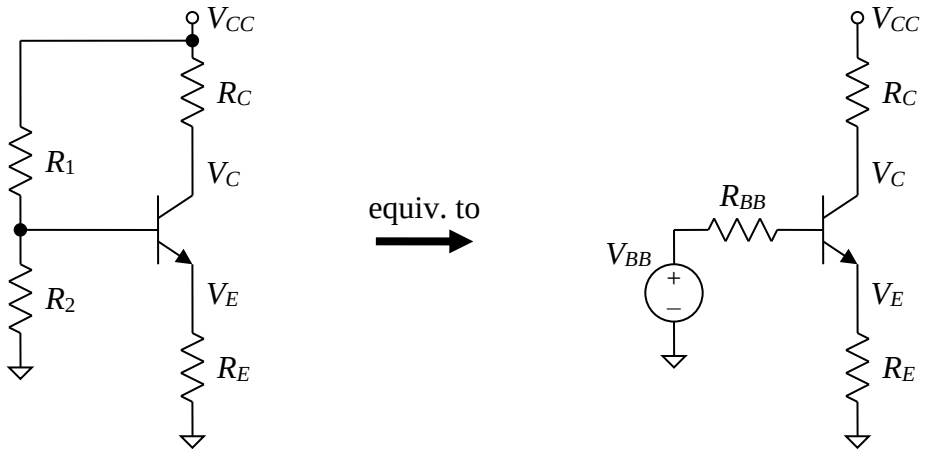
General analysis techniques for BJT circuits

- determination of region of operation (cutoff, active, or saturation)
  - try to determine whether base-emitter junction is forward biased if possible; helps to rule out (or not) cut-off region
  - assume BJT is in one region and analyze the circuit based on that assumption
  - check all voltages and currents and determine whether their values are consistent with the initial assumption. If so, analysis is complete. If not, use the results of the initial analysis to determine likely region of operation. Repeat analysis under new assumption and confirm.
- v_{CE} (for *npn* BJTs) is always positive (negative for *pnp*; i.e., v_{EC} is positive for *pnp*)
- $v_{BE} \approx 0.7$ V (for Si *npn*) in the active and saturation regions
- cut-off region: $i_B = i_C = 0$ and $v_{BE} < 0.7$ V (for Si *npn*)
- active region: $v_{BE} \approx 0.7$ V, $i_C = \beta i_B$ and $v_{CE} > v_{CE}|_{\text{sat}} \approx 0.2$–$0.3$ V (for Si *npn*)
- saturation region: $v_{BE} \approx 0.7$ V, $i_C < \beta i_B$ and $v_{CE} = v_{CE}|_{\text{sat}} \approx 0.2$–$0.3$ V (for Si *npn*)
- for more accurate analysis (rarely necessary), use
  $i_B = I_{SB} e^{v_{BE}/\eta V_T}$ and $i_C = \beta I_{SB} e^{v_{BE}/\eta V_T}$,
  where I_{SB} = saturation (or scale) current for B-E junction, η = emission coefficient (typically assumed to equal one), and V_T = thermal voltage

BJT inverter (common-emitter amplifier)

- can be used as a logical NOT gate (but not a very good one)
- transfer characteristic (v_o vs. v_{in}) has negative slope in active region and nearly zero slope in cut-off and saturation regions
- transfer characteristic in active region is not actually linear because of exponential relationship between i_B and v_{BE} (and therefore also between i_C and v_{BE}).
- determination of the actual nonlinear transfer characteristic requires the solution of a transcendental equation. The Lambert W and Wright Omega functions can be used.

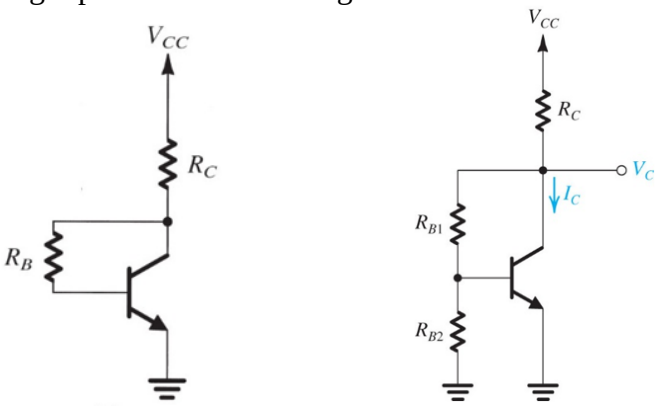
BJT biasing circuit with emitter degeneration resistor



- for analysis purposes, can replace base biasing network with a Thévenin equivalent circuit (TEC) with $V_{BB} = V_{CC}\dfrac{R_2}{R_1 + R_2}$ and $R_{BB} = R_1 \| R_2$; simplifies evaluation of I_B
- using TEC above, for unipolar power supply, in the active region the quiescent collector current is given by
  $I_C \approx \dfrac{V_{BB} - V_{BE}}{R_{BB}/\beta + R_E}$ (*npn*)
- *pnp* bias analysis is slightly different; for unipolar power supply, in the active region the quiescent collector current is given by
  $I_C \approx \dfrac{V_{CC} - V_{BB} - V_{BE}}{R_{BB}/\beta + R_E}$ (*pnp*)
- design for quiescent output voltage, quiescent collector current, and/or quiescent voltage drop across emitter resistor (if present)
- BJTs are usually biased for operation in the active region when used as amplifiers
- the parameter β has strong temperature dependence and device variation
- negative feedback via emitter degeneration resistor (R_E) stabilizes I_C
- current through R_1 and R_2 is typically designed to be 0.1 to 1 times I_E (or 10–100 times I_B); upper end of that range is excessive in most cases
- resistors R_1 and R_2 do not behave as a true voltage divider because $I_B \neq 0$; however, they approximate a voltage divider because I_B should be small compared to current through R_1 and R_2 (1/10 or less)
- trade-off: higher current through R_1 and R_2 leads to more stable quiescent point but lower input resistance and higher current demand from power supply
- common design rule of thumb: $I_C R_C = I_E R_E = \dfrac{1}{3}V_{CC}$, although the voltage across R_E is sometimes designed to be less than this (e.g., if V_B, not V_E, is set to $V_{CC}/3$)
- DO NOT ASSUME THAT $V_E = (1/3)V_{CC}$ FOR <u>*ANALYSIS*</u> CASES! It might have been given a different value during its *design*.
- variation for bipolar (pos./neg.) power supplies: use R_E and R_C but only a single resistor (R_B) from base to ground

Alternative biasing circuits

- can use collector-to-base feedback resistor as shown below
- variation below right provides an extra degree of freedom to control V_C as well as I_C

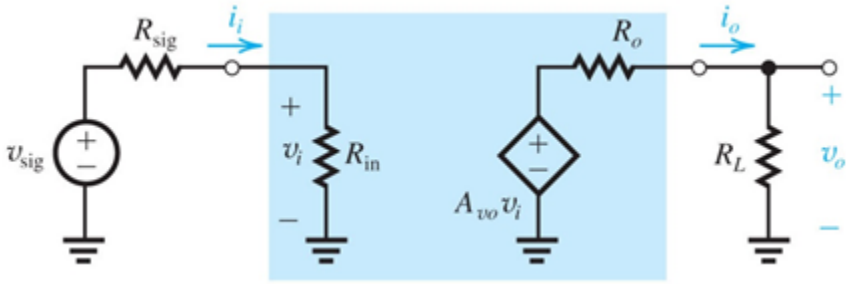


Sources: (left) Sedra & Smith, *Microelectronic Circuits*, 7th ed., 2015, p. 466. (right) p. 496.

General small-signal modeling concepts

- definition of small signal (sometimes called "incremental signal")
- separation of bias considerations (quiescent levels; output voltage swing range) from small-signal considerations (gain, input and output resistance)
- replacement of DC voltage sources with short circuits (because the voltage across a DC voltage source cannot change with time, signal voltage across DC voltage source = 0)
- replacement of DC current sources with open circuits (because the current through a DC current source cannot change with time, signal current through DC current source = 0)
- in practice, DC voltage sources are typically bypassed at AC (i.e., at signal frequency) using capacitors; DC current sources are sometimes bypassed as well
- small-signal model of BJT is valid only when device operates in the active region but not in cut-off or saturation regions
- small-signal model of FET is valid only when device operates in the saturation region but not in cut-off or triode regions
- derivation of small-signal voltage gain
- difference between open-circuit gain A_{vo}, amplifier gain A_v, and overall gain G_v
- derivation of small-signal input resistance R_{in}; test source usually necessary
- derivation of small-signal output resistance R_{out}; test source usually necessary
- R_{in} or R_{out} can be thought of as resistance "looking into" a particular pair of terminals from the source or load
- R_{in} analysis: remove TEC of signal source but keep R_L
- R_{out} analysis: remove R_L but keep R_{sig} (Thévenin/Norton equiv. resistance) of signal source and set Thévenin equiv. voltage or Norton equiv. current to zero
- simplifications in gain/resistance expressions when one term is much greater/smaller than another term
- calculation or approximation errors of less than a few percent usually of no concern

Two-port amplifier representation (refer to diagram below) using Thévenin equivalent circuits



Source: Sedra & Smith, *Microelectronic Circuits*, 7th ed., 2015, p. 425.

- v_i (or v_{in}) and v_o are the voltages measured at the amplifier's input and output terminals; note that in general v_{in} is not the same as v_{sig}
- a set of input or output terminals is sometimes called a "port"
- input port of amplifier has an equivalent input resistance R_{in}
- A_v = voltage gain with finite-resistance load; A_{vo} = "open-circuit" voltage gain ($R_L \rightarrow \infty$)
- "no-load" gain assumes that $R_L \rightarrow \infty$, not $R_L = 0$ (if the load is missing, it leaves an open circuit at the output port)
- output port of amplifier can be represented as a Thévenin equivalent circuit with dependent voltage source $A_{vo}v_{in}$ and output resistance R_o (sometimes labeled R_{out})
- relationship between source resistance R_{sig} and input resistance R_{in} required to maximize input voltage, current, or power to amplifier
- relationship between output resistance R_o (sometimes labeled R_{out}) and load resistance R_L required to maximize output voltage, current, or power from amplifier

Small-signal modeling of BJT circuits

- small-signal models of BJT: hybrid-pi model and T model
- small-signal condition: $|v_{be}| << \eta V_T$,
  where η = emission coefficient ($\eta = 1$ usually assumed); and V_T = thermal voltage, related to temperature T in kelvins by $V_T = T/11{,}600$
- incremental base-emitter resistance r_π and what it represents (finite slope of i_B-v_{BE} characteristic of base-emitter *pn*-junction, which obeys diode equation):
  $$r_\pi = \frac{\eta V_T}{I_B} = \frac{\beta \eta V_T}{I_C} = \frac{\beta}{g_m} = r_e(\beta + 1)$$
- incremental collector-emitter resistance r_o (called transistor output resistance in the textbook and "Early resistance" by us) and what it represents (non-zero slope of i_C-v_{CE} characteristic in the active region); typically, r_o = 50 kΩ or more for BJTs
- relationship between small-signal output port resistance r_o (collector-emitter resistance) and Early voltage (V_A):
  $$r_o \approx \frac{V_A}{I_C}$$
- dependence of g_m of BJT on quiescent collector current I_C:
  $$g_m = \frac{I_C}{\eta V_T}$$
- relationship between α and β (where $I_C = \alpha I_E$):
  $$\alpha = \frac{\beta}{\beta + 1}$$

- emitter resistance r_e in T model of BJT:

$$r_e = \frac{\alpha}{g_m} = \frac{r_\pi}{\beta + 1}$$

- derivation of g_m from i_C vs. v_{BE} equation (diode eqn applied to B-E junction)
- effect of emitter degeneration resistor (R_E) on gain and input resistance
- effect of "amount of negative feedback" ($1 + g_m R_E$) on peak allowable input voltage in CE amplifiers with emitter degeneration and its derivation (also applies to emitter followers, but R_E is replaced with $R_E||R_L$)
- typical values of important BJT and circuit parameters such as β, r_o, bias resistor values, and saturation voltage
- *pnp* small-signal model: directions of i_b and βi_b and polarity of v_{be} are the same as for *npn* model (note that these are SMALL-SIGNAL quantities; directions and polarities of BIAS voltages and currents are mostly different for *npn* and *pnp*)
- data sheet notation: $h_{FE} = \beta$; $h_{fe} = \beta$; $h_{ie} = r_\pi$; $h_{oe} = 1/r_o$ (old h-parameters)

Basic amplifier design process

- identify most restrictive specifications
- use analysis to derive relationships between component and device parameters (i.e., quantities like β and resistor values) and specified performance requirements such as gain and input/output resistance
- look for quantities that dominate other quantities in sums and quotients and especially ways to minimize effects of variable β for BJTs or k_n and V_t for MOSFETs
- design bias network to adjust g_m, swing range, and other parameters to satisfy specifications
- select capacitor values, bypass arrangements, etc. to meet remaining specifications or to confirm that minimum performance requirements will be met
- choice of input/output DC blocking capacitor values: reactance should not necessarily be << smallest resistance in series with it; it should only be small enough not to affect gain. Classic example: if R_{sig} is small and R_{in} is large, do not make $|X_C| << R_{sig}$. It is usually enough to make $|X_C| << R_{in}$. This allows the smallest possible capacitance to be used.

<u>Relevant course material:</u>

Homework: #1, #2, and #3
Labs: #1 and #2
Readings: Assignments from Jan. 17 through Feb. 7, including the supplemental reading: "Small-Signal Analysis of PNP Emitter Follower"

This exam will focus primarily on the course outcomes list below and related topics such as biasing:

1. Apply an appropriate small-signal model to analyze properties such as gain and input/output impedance of a BJT or MOSFET amplifier.

The course outcomes are listed on the Course Policies and Information sheet, which was distributed at the beginning of the semester and is available on the Syllabus and Policies page at the course web site. The outcomes are also listed on the Course Description page. Note, however, that some topics not directly related to the course outcomes could be covered on the exam as well.