ECEG 351 **Electronics II** **Spring 2024**

Policies and Review Sheet for Exam #3

The following policies will be in effect for the exam. They will be included in a list of instructions and policies on the first page of the exam:

1. You will be allowed to use a non-wireless enabled calculator, such as a TI-89.
2. You will be allowed to use three 8.5 × 11-inch two-sided handwritten help sheets. No photocopied material or copied and pasted text or images are allowed. If there is a table or image from the textbook or some other source that you feel would be helpful during the exam and that is not included on the table and formula sheet that I will provide, please notify me.
3. All help sheets will be collected at the end of the exam but will be returned to you later.
4. If you begin the exam after the start time, you must complete it in the remaining allotted time. However, you may not take the exam if you arrive after the first student has completed it and left the room. The latter case is equivalent to missing the exam.
5. **You may not leave the exam room without prior permission except in an emergency or for an urgent medical condition. Please use the restroom before the exam.**

The exam will take place 8:00–9:50 am on Thursday, April 11 in Breakiron 065.

The following is a list of topics that could appear in one form or another on the exam. Not all of these topics will be covered, and it is possible that an exam problem could cover a detail not specifically listed here. However, this list has been made as comprehensive as possible. **You should be familiar with the topics on the review sheet for the previous exam as well.**

Although significant effort has been made to ensure that there are no errors in this review sheet, some might nevertheless appear. The textbook and the supplemental readings are the final authority in all factual matters, unless errors have been specifically identified there. You are ultimately responsible for obtaining accurate information when preparing for the exam.

Capacitance and inductance in electronic circuits

- stray capacitance
    - between leads (individual wires, or wires in cables)
    - due to interconnecting wires/cables
    - between circuit board pads or pads and ground plane or other ground points
    - between nodes in integrated circuits
    - between integrated circuit pins
    - typically has values measured in pF or less
    - must be considered in HF range (3–30 MHz) and above; very serious issue in microwave and millimeter wave circuits
- stray inductance
    - due to wire or circuit board trace loops (any loop in a circuit)
    - due to interconnecting wires/cables
    - mutual inductance between circuit loops
    - typically has values measured in nH or less
    - must be considered in HF range (3–30 MHz) and above; very serious issue in microwave and millimeter wave circuits

The decibel (dB) unit

- definition: gain in dB $= 10\log\frac{P_o}{P_i} = 10\log\frac{v_o^2}{v_i^2} = 20\log\frac{v_o}{v_i} = 20\log\frac{i_o}{i_i}$
- technically, voltage/current ratios can only be used when $R_{in} = R_L$, but this restriction is often ignored in practice
- distinction between use with power ratios and voltage/current ratios
- $\log\frac{a}{b} = \log a - \log b$ and $\log ab = \log a + \log b$
- $|j| = 1$; $\log(0) = -\infty$; $\log(1) = 0$
- 0 dB ≠ 0 W or 0 V or 0 A! It means no change in power or voltage/current (i.e., ×1)
- 3 dB = power increase of ×2; voltage/current increase of ×1.414
- 6 dB = power increase of ×4; voltage/current increase of ×2
- 10 dB = power increase of ×10; voltage/current increase of ×3.16
- 20 dB = power increase of ×100; voltage/current increase of ×10
- −3 dB = power decrease of ×0.5; voltage/current decrease of ×0.707
- −10 dB = power decrease of ×0.1; voltage/current decrease of ×0.316
- −20 dB = power decrease of ×0.01; voltage/current decrease of ×0.1

Bode plots

- plot of gain in dB and/or phase vs. frequency with frequency on a log scale
- definitions of “decade” and “octave”
- identification of zeros and poles in transfer functions
- each zero in transfer function contributes +20 dB/decade rise in gain vs. log *f* at frequencies well above the zero
- don’t forget the zeros at DC in high-pass characteristics (accounts for low-freq. roll-off)
- each pole contributes –20 dB/decade drop in gain vs. log *f* at frequencies well above the pole
- each zero contributes a +90° change in phase, and each pole contributes –90° change in phase well above zero/pole
- exactly at the zero/pole frequency, the phase change is ±45° (except in the case of a zero at $\omega = 0$; it contributes +90° beginning at $\omega = 0$); if there are multiple zeroes/poles at the same frequency, then the phase change is the appropriate multiple of ±45°
- 20 dB/decade is equivalent to 6 dB/octave

Approximation of cut-off frequencies that bracket midband region

- high-frequency cut-off: $\omega_H \approx \omega_1 \| \omega_2 \| \omega_3 \| \cdots$ or $f_H \approx f_1 \| f_2 \| f_3 \| \cdots$
- low-frequency cut-off: if one frequency is clearly dominant,
  $\omega_L \approx \omega_a + \omega_b + \omega_c + \cdots$ or $f_L \approx f_a + f_b + f_c + \cdots$
- if two or more low-frequency poles are dominant, $f_L \approx \sqrt{f_a^2 + f_b^2 + f_c^2 + \cdots}$

Frequency response of circuits containing capacitors

- high-pass vs. low-pass characteristics
- approximation of transfer function using standard representations of zeros and poles
- typical high-freq caps
  - internal junction capacitances of BJTs and FETs
  - capacitors that shunt input or output node to signal ground
  - capacitors between output and input nodes (transverse or feedback capacitances)
  - many stray capacitances
  - most capacitances in parallel with loads, such as cable capacitance (shunts output node to ground)

- typical low-freq caps
    - capacitors in series with the signal path (in series with input/output nodes)
    - capacitors that shunt the common terminal of a BJT or FET to signal ground (such as the base capacitor in a common-base amplifier); gate bias bypass capacitor (often labeled C_G) in common-gate MOSFET amp is an exception
- typical "unimportant" caps: power supply bypass capacitors (no effect on freq. response)
- determination of dominant low and high-frequency poles by the Thévenin equivalent resistance method
    - classify each capacitor as high-freq, low-freq, or "unimportant" (irrelevant)
    - select one capacitor
    - in the small-signal model, short all other low-freq capacitors and open all other high-freq capacitors
    - set all independent voltage and current sources to zero (short voltage sources and open current sources)
    - leave dependent sources in the circuit unaltered
    - find the small-signal Thévenin equivalent resistance seen by the capacitor under consideration
    - find the "candidate" pole frequency associated with that capacitor
    - repeat the steps above (except the first) for each capacitor in circuit
    - after calculating all of the candidate pole frequencies, find the upper and lower cut-off frequencies using the appropriate approximation
    - beware: input capacitances of oscilloscopes (or other measuring devices) can sometimes introduce dominant high-frequency poles
    - short-circuit time constant method is equivalent to sum of low-freq poles
    - open-circuit time constant method is equivalent to "parallel" combo of high-freq poles

Design process to set lower cut-off frequency with minimum total capacitance

- find smallest associated equivalent resistance of all low-freq. capacitors
- use that capacitor to set the dominant pole f_L
- select remaining capacitor values so that their poles are less than $0.05f_L$ or so
- alternative method:
    - "distribute" f_L among capacitors by percentages
    - assign at least 80% (90% is better) to the capacitor with the smallest associated equivalent resistance
    - distribute percentage balance among remaining capacitors
    - can nudge percentages up or down a little to obtain standard values for capacitors

Internal capacitances in BJTs

- depend on forward or reverse-bias conditions
- collector-base junction (reverse-biased) capacitance C_μ is typically a few pF and depends on V_{CB} (quiescent collector-base voltage)
- base-emitter junction (forward-biased) capacitance C_π can be tens to hundreds of pF or more and depends on quiescent collector current
- common-emitter short-circuit current gain (β_0 is the DC value):

$$\beta(\omega) = \frac{\beta_0}{1 + j\omega r_\pi \left(C_\pi + C_\mu\right)}$$

- unity-gain bandwidth or transition frequency:

$$f_T = \frac{g_m}{2\pi\left(C_\pi + C_\mu\right)}$$

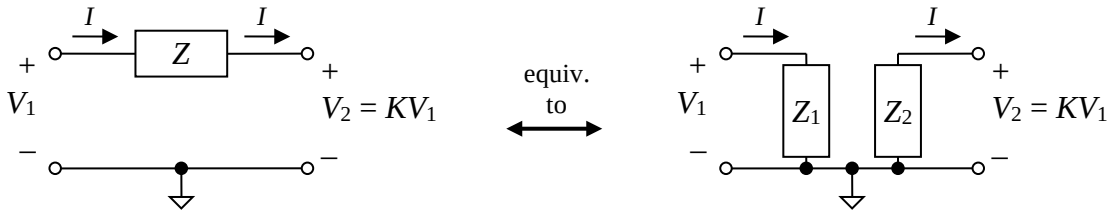
Impact of inductors in combination with capacitors on biasing and frequency response

- inductors act as shorts at DC (zero frequency)
- *total* voltage (bias + signal) at some nodes in circuit can rise above V_{CC} (or V_{DD})
- impedance of inductor = $j\omega L$; reactance = ωL
- presence of inductor(s) can lead to complex conjugate pole pairs; three possibilities:
    - two real distinct poles (i.e., at different frequencies)
    - two real identical poles (i.e., at the same frequency)
    - pair of complex conjugate poles
- complex conjugate pole pair can lead to a peak in the gain magnitude Bode plot at the resonant frequency associated with an LC pair (series or parallel resonance)
- designers often avoid inductors (larger, heavier, and more expensive than capacitors of similar reactances), tend to have significant stray reactances (e.g., inter-winding capacitance, wire resistance)
- inductors (and transformers) are vitally important in many RF/wireless/microwave circuits, where advantages of employing inductors outweigh disadvantages

Miller's Theorem, Miller effect, and Miller multiplication

- applies to input/output circuit nodes bridged by a transverse impedance Z (see figure below) with voltage gain K between nodes
- allows bridging (transverse) impedance to be replaced by equivalent impedances between each node and ground for analysis purposes:

$$Z_1 = \frac{Z}{1-K} \quad \text{and} \quad Z_2 = \frac{Z}{1-1/K} = \frac{KZ}{K-1}$$



- practical implication: if the voltage multiplying factor K (usually a voltage gain) is very large, then the equivalent shunt impedance Z_1 on low-voltage (V_1) side is smaller than Z by roughly the same factor
- if Z is a capacitor and K is negative, its capacitance value is roughly multiplied by $|K|$ on the low-voltage (input, or V_1) side; this is Miller multiplication
- if Z is a resistor and K is a large negative value, the input resistance of the circuit is greatly reduced
- CB amps, CG amps, emitter followers, source followers, and diff amps are all relatively immune to Miller multiplication of BJT/MOSFET internal capacitances
- Miller effect can sometimes be used to advantage. Examples: "bootstrapping" in emitter/source followers to increase input impedance, negative impedance converters (typically used to make capacitors act like inductors)

Relevant course material:

HW: #7, and #8
Labs: #4
Reading: Assignments from Mar. 6 through Apr. 5, including the supplemental reading
"The Miller Effect in Various Amplifier Topologies" (slides)
Justification of Short-Circuit Time Constant Method for Amplifier Frequency Response

This exam will focus primarily on course outcomes #3 through #5 (given below) and related topics.

4. Analyze the frequency response of a basic BJT or MOSFET amplifier.
5. Select components to achieve a specified lower cut-off frequency for a BJT or MOSFET amplifier.

The course outcomes are listed on the Course Policies and Information sheet, which was distributed at the beginning of the semester and is available on the Syllabus and Policies page at the course web site. The outcomes are also listed on the Course Description page. Note, however, that some topics not directly related to the course outcomes could be covered on the exam as well.