ECEG 351 **Electronics II** **Spring 2024**

Homework Assignment #4 – due via Moodle at 11:59 pm on Friday, Feb. 23, 2024

***Instructions, notes, and hints*:**

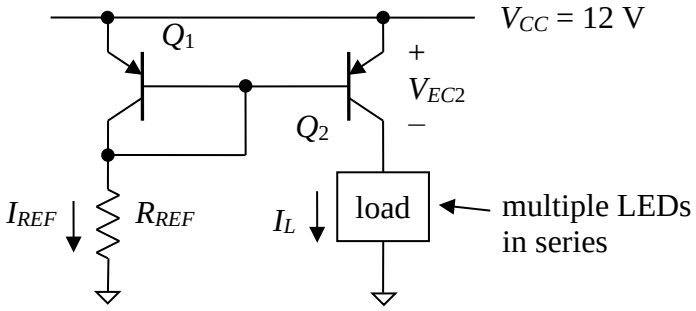
You may make reasonable assumptions and approximations to compensate for missing information, if any. Provide the details of all solutions, including important intermediate steps. You will not receive credit if you do not show your work.

Unless otherwise specified, you may assume that all BJTs are at room temperature, the emission coefficient $n = 1$, $V_{BE} = 0.7$ V (quiescent value), and $V_{CE}|_{sat} = 0.2$ V. If the Early voltage V_A is not specified, you may ignore its effects. For now, unless otherwise specified, capacitors can be assumed to have values large enough that they act as shorts at the operating frequency.

The first set of problems will be graded and the rest will not be graded. Only the graded problems must be submitted by the deadline above. Do not submit the ungraded problems.

***Graded Problems*:**

1. The *pnp*-based current mirror circuit shown below is to be used to drive a load consisting of a set of series-connected white LEDs, each of which has a turn-on voltage of roughly 2.8 V. Constant-current sources are often used in LED lighting systems since the light output is directly related to the LED current. Find the standard 5% value that R_{REF} should have to make I_L approximately equal to 20 mA. Also find the maximum number of series-connected LEDs that can be supplied with the proper operating current by the mirror. Assume that the two BJTs are matched; that is, they have the same junction area, the same doping levels, etc. Also assume that $\beta = 80$ to 150, $V_{EB} = 0.7$ V, and $|V_A| = 80$ V, although the Early effect can be neglected during the design phase. Note that if 5% precision resistors are used, then the precision of the output current can be expected to be no better than roughly 5%.



2. The relationship between the reference current I_{REF} and load current I_L for a Widlar current source is given by the expression shown below. Assuming that $V_{CE}|_{sat} = 0.2$ V, find the maximum ratio I_{REF}/I_L for which the compliance limit of the Widlar source is no more than 0.3 V.

$$I_L R_E = nV_T \ln\left(\frac{I_{REF}}{I_L}\right)$$

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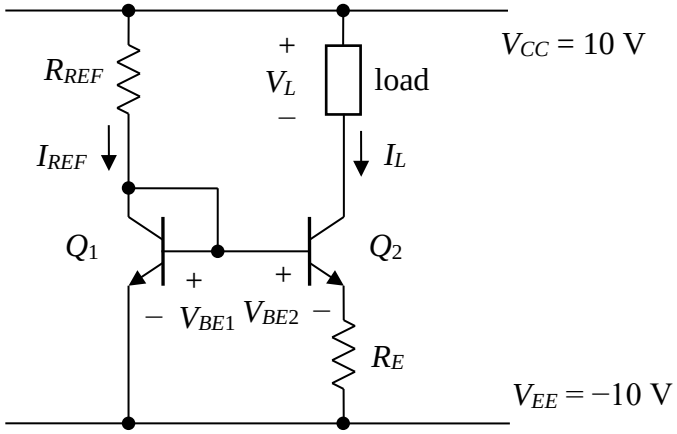
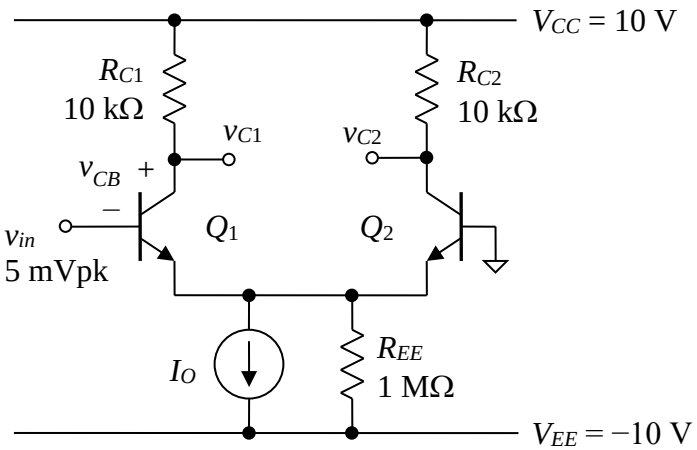
3. Shown below is a Widlar current source that will supply a constant current to an unknown load. Assume that Q_1 and Q_2 are identical and that $\beta = 150$, the Early voltage $V_A = 50$ V, the scale current $I_{SB} = 10^{-17}$ A for the B-E junction, the emission coefficient $\eta = 1$, and the thermal voltage $V_T = 25$ mV for both BJTs. Find:

- **a.** the values of R_{REF} and R_E necessary to provide a current of 25 μA to the load using a reference current of 2.0 mA.
- **b.** the actual values of V_{BE1} and V_{BE2} (not the approximate value 0.7 V).
- **c.** the Norton equivalent resistance R_{EE} of the mirror. Use Equation (8.105) in Sec. 8.7.4 of the textbook (Sedra & Smith, 8th ed.)
- **d.** the compliance limit V_{comp}.



4. In the BJT diff amp circuit shown below, a sinusoidal signal with a peak amplitude of 5 mV is applied to the single-ended input; that is, v_{in} varies from −5 mV to + 5 mV. The quiescent base voltage of Q_1 is 0 V. The output resistance R_{EE} of the current mirror is high enough that it can be ignored. The BJTs can be kept well out of the saturation region by ensuring that the total collector-base voltage v_{CB} never drops below 0 V. Find an appropriate limit on the value of mirror current I_O to ensure that v_{CB} is greater than 0 V for the specified input signal limits. Note that you must consider the *total* (quiescent plus signal) voltages and currents to solve the problem properly, and you must find the single-ended differential-mode voltage gains $A_{d\text{-}se1} = v_{c1}/v_{in}$ and $A_{d\text{-}se2} = v_{c2}/v_{in}$ that correspond to the value of I_O. You may assume that $\alpha \approx 1$, where $\alpha = \beta/(\beta + 1)$. For the BJTs, $V_{BE}|_{on} = 0.7$ V, $V_{CE}|_{sat} = 0.3$ V, $\beta = 150$, $n = 1$, and $V_T = 25$ mV. You may ignore the Early effect (i.e., $r_o \to \infty$).



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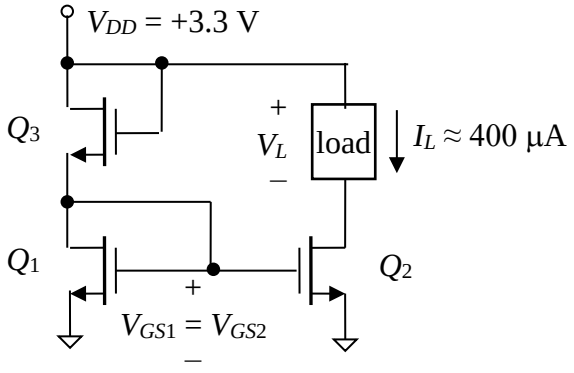
5. For the diff amp circuit considered in the previous problem, the quiescent emitter current is equal to $0.5I_O$, assuming that the tiny current that flows through R_{EE} is negligible. Find the value that v_{in} must have to make the emitter current in Q_2 (I_{E2}) rise to a value 30% higher than its quiescent value. You do not need to know the value of I_O to solve this problem. Note that the small-signal condition is probably not satisfied in this case. Assume the same operating conditions and BJT parameters as for the previous problem.

6. Design the MOSFET-based current mirror circuit below to sink a nominal current of 400 μA through the attached load. The MOSFETs are to be fabricated using the 0.5 μm process technology. (See Appendix K of Sedra & Smith, 8th ed., available at the ECEG 351 Moodle site, for a list of typical parameter values associated with various process technologies.) Set the channel length L of all transistors equal to the process length 0.5 μm, and set the width of Q_2 to provide an overdrive voltage V_{OV} of 0.5 V. The sink current I_L and reference current I_{REF} (through Q_3 and Q_1) should be matched, at least nominally. The Early voltage V_A must be determined from data available in the process technology table in Appendix K.

- **a.** Find the required values of the channel widths W_1, W_2, W_3 and voltage V_{GS2} (which equals V_{GS1}) to meet the specifications. You may ignore the channel length modulation effect.
- **b.** Determine the compliance limit V_{comp} of the mirror circuit.
- **c.** Find the Norton equivalent output resistance of the current mirror seen by the load.
- **d.** Find the change in load current I_L that results from a +0.5 V change in V_L.



***Ungraded Problems*:**

The following problems will not be graded. However, you should attempt to solve them on your own and then check the solutions. Try not to give up too quickly if you struggle to solve any of them. Move on to a different problem and then come back to the difficult one after a few hours.

1. For the Widlar current source shown on the next page, find the reference current I_{REF} and the load current I_L. You will have to solve a transcendental equation to find I_L, which will likely require a trial-and-error approach unless your calculator is capable of solving that type of problem. Try an initial reasonable guess (or two) and then use the error obtained when you evaluate the applicable equation to guide you to the next guess. The BJTs are matched with β = 150, V_A = 50 V, scale current $I_{SB} = 10^{-17}$ A for the B-E junction, η = 1, and V_T = 25 mV.

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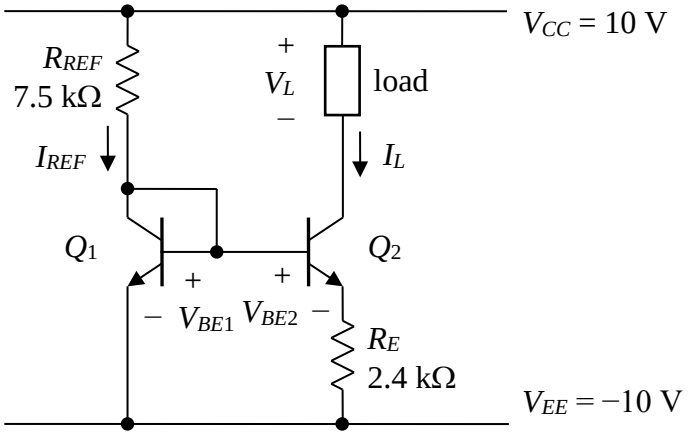
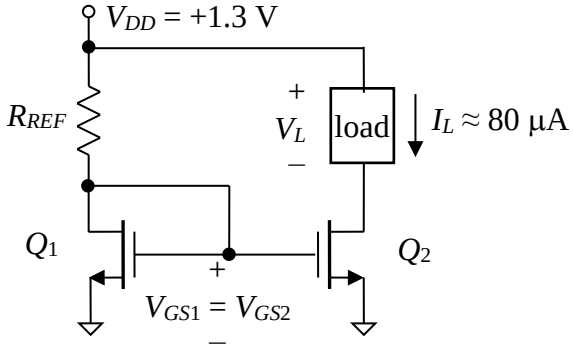
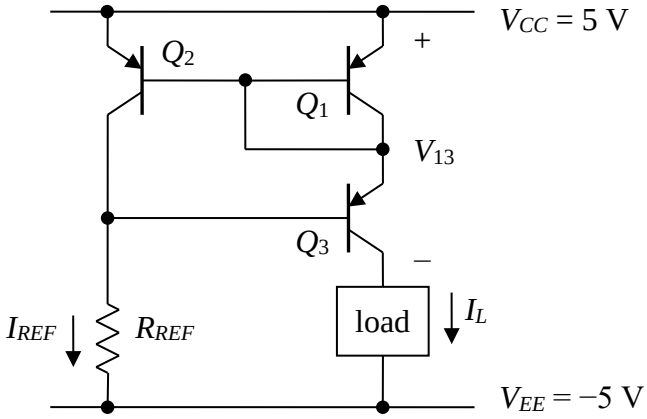


Circuit for Ungraded Problem 1.

2. Sketch the PMOS counterpart of the mirror circuit shown below. In the new circuit, Q_1 and Q_2 are matched with $|V_{tp}| = 0.4$ V and $\mu_p C_{ox} = 80\ \mu\text{A/V}^2$. Find the device W/L ratios and value of R_{REF} required to set $I_L \approx 80\ \mu$A. The mirror is required to operate for V_L as high as 1.1 V. Neglect the channel-length modulation effect.



3. Shown below is a Wilson current mirror made from *pnp* BJTs. Assume that the BJTs are matched and have $\beta = 100$ and $|V_A| = 40$ V. Find the standard 5% value that R_{REF} should have to make I_L approximately equal to 750 μA if V_{13} (equal to $V_{EC1} + V_{EC3}$) is at the compliance limit. Assume that $V_{EB} \approx 0.7$ V and that the Early effect can be neglected at the compliance limit. If 5% precision resistors are used, then the precision of the output current does not have to be any better than 5%.



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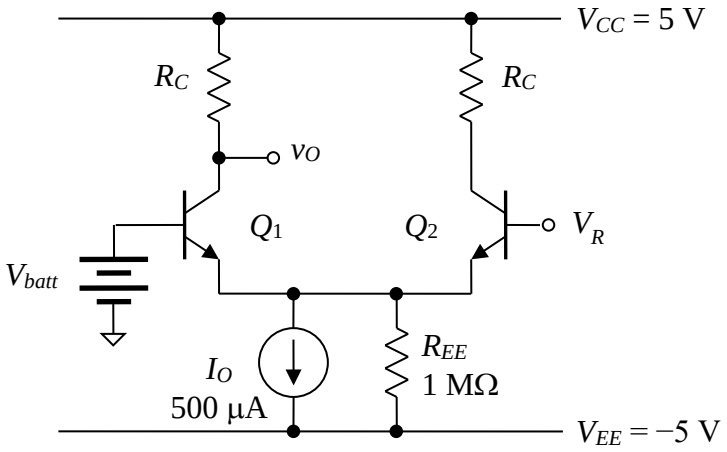
4. For the Wilson mirror designed in the previous problem:

- **a.** Estimate the total power dissipated by the mirror circuit (not including the load but including R_{REF}) at the compliance limit. You may neglect the power dissipated in the base-emitter junctions (i.e., all dissipations found via $I_B V_{EB}$).
- **b.** Find the numerical value of the overall small-signal output resistance of the mirror seen by its load. Include the Early effect. You may use the textbook's equation for output resistance.
- **c.** Taking the Early effect into account, find the output current I_L of the mirror when the load has equivalent resistances of 1 kΩ, 5 kΩ, and 9 kΩ. Tabulate the results. Assume that I_L = 750 μA exactly when the mirror is at its compliance limit. Note that you will have to determine the Norton equivalent current I_O of the mirror before you can find I_L. Assume that V_{EC} = 0.2 V at the edge of the saturation region and that V_{EB} = 0.7 V.

5. The circuit shown below is meant to monitor the output voltage of a AA battery that has a nominal voltage V_{batt} of around 1.5 V when it is new. The battery voltage declines as it is used and drops quickly when the battery is almost fully discharged. Voltage V_R applied to the base of Q_2 is a DC reference voltage and is generated by circuitry not shown in the diagram. A very high impedance voltmeter is connected between the v_O node and ground. Find the required values of V_R and the collector resistors R_C so that the output voltage v_O is close to 0 V when the battery voltage is greater than approximately 1.4 V and close to V_{CC} when the battery voltage drops to a value less than approximately 1.2 V. For the BJTs, you may assume that $V_{BE}|_{on}$ = 0.7 V, $V_{CE}|_{sat}$ = 0.3 V, and β = 150. The Early effect can be ignored (i.e., $r_o \to \infty$). You may assume that the emission coefficient η = 1 and the thermal voltage V_T = 25 mV. *Hint*: Carefully read Sec. 9.2.3 in Sedra & Smith, 7th ed.



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6. The BJT diff amp shown below is to have collector resistors of 40 kΩ each and a differential-mode gain A_d (equal to v_{od}/v_{id}) of 240 V/V at room temperature. The current mirror has an output resistance R_{EE} that is so large that it can be ignored for most analysis tasks. Input voltage v_{id} is a small time-varying signal with zero average value. Assume that $\eta = 1$ (emission coefficient), $V_{BE} = 0.7$ V (quiescent value), $V_{CE}|_{sat} = 0.2$ V, and that the Early effect can be ignored. Also assume that the quiescent values of the two base voltages are kept at zero by additional circuitry not shown in the diagram. The common-mode and differential-mode input voltages can be modeled as shown next to the circuit diagram.

a. Find the current mirror value I_O required to achieve the stated gain.
b. Find the minimum value that V_{CC} can have to ensure that the quiescent collector voltages of Q_1 and Q_2 are each at least 1.0 V.
c. If the differential input voltage v_{id} is sinusoidal, find the maximum peak value (amplitude) that it can have to ensure that Q_1 and Q_2 each operate in the active region at all times. Remember that you need to consider both the quiescent (bias) and signal voltage levels to determine total voltages. This includes the total emitter voltage.