ECEG 351 **Electronics II** **Spring 2024**

Homework Assignment #6 – due via Moodle at 11:59 pm on Friday, Mar. 8, 2024

***Instructions, notes, and hints*:**

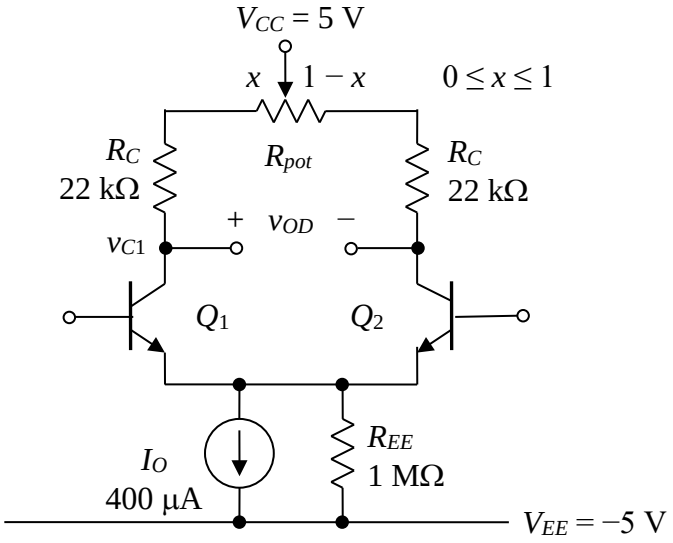
You may make reasonable assumptions and approximations to compensate for missing information, if any. Provide the details of all solutions, including important intermediate steps. You will not receive credit if you do not show your work.

Unless otherwise specified, you may assume that all BJTs are at room temperature, the emission coefficient $\eta = 1$, $V_{BE} = 0.7$ V (quiescent value), and $V_{CE}|_{sat} = 0.2$ V. If the Early voltage V_A is not specified, you may ignore its effects. For now, unless otherwise specified, capacitors can be assumed to have values large enough that they act as shorts at the operating frequency.

The first set of problems will be graded and the rest will not be graded. Only the graded problems must be submitted by the deadline above. Do not submit the ungraded problems.

***Graded Problems*:**

1. Determine the minimum value of the potentiometer R_{pot} in the circuit shown below required to allow cancellation of an input offset voltage V_{OS} of up to ±5 mV caused by a mismatch in the junction areas of the two BJTs. The two collector resistors have been laser trimmed so that the difference in their values is insignificant. The average value of β is 200. If you need a value for α [equal to $\beta/(\beta + 1)$], you may use the average value. The value of R_{EE} is large enough that its effect on the input offset voltage (and the compensation of V_{OS}) can be ignored. The resistance between the wiper of the potentiometer and its left terminal is xR_{pot}, and the resistance between the wiper and the right terminal is $(1 - x)R_{pot}$. You may ignore the Early effect in Q_1 and Q_2. *Hint*: It might be helpful to read the definitions of I_S (the scale or saturation current) found on p. 162 and p. 311 of the textbook (Sedra & Smith, 8th ed., Sec. 6.1.2). The latter definition is the more useful one in the context of BJTs.



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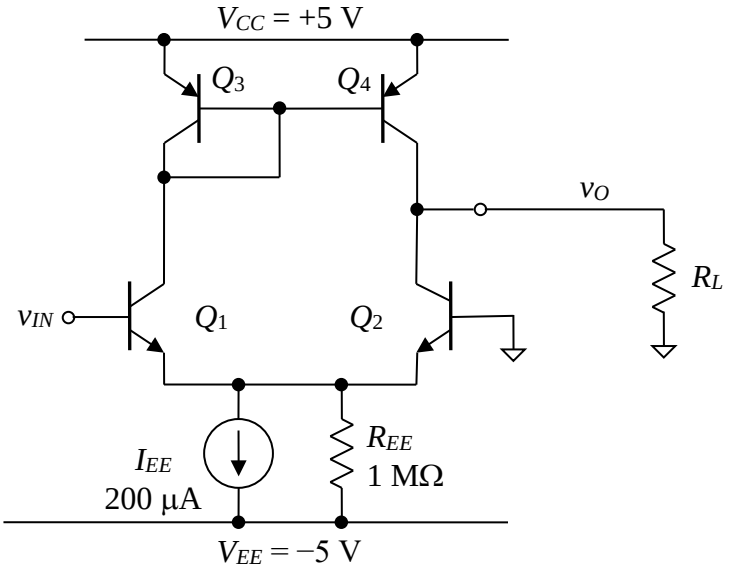
2. This problem examines a practical issue that must be considered when testing diff amps with current mirror loads. As shown below, a load resistance R_L has been connected to the output node of a diff amp for test purposes. The value of R_{EE} is large enough that its effect on the quiescent bias currents can be ignored. Q_1 and Q_2 have V_A = 50 V, β = 200, and $V_{CE}|_{sat}$ = 0.2 V. Q_3 and Q_4 have V_A = 50 V, β = 100, and $V_{EC}|_{sat}$ = 0.2 V. Account for the Early effect for small-signal analysis, but ignore it for large-signal and bias analyses. You will need to understand the material covered in Sec. 9.5 of the textbook (Sedra & Smith, 8th ed.) and the related lecture material to solve this problem. Find:

- **a.** An expression for the small-signal voltage gain with a finite load resistance R_L present.
- **b.** The maximum value that R_L can have to ensure that Q_2 and Q_4 operate in the active region even if $|v_{IN}| > 4nV_T$.
- **c.** Comment on how the results of parts a and b place conflicting pressures on the selection of a value for R_L.



3. [adapted from Prob. 9.97 of Sedra & Smith, 8th ed.] BJT diff amps with current mirror loads suffer from a systematic offset voltage effect. It occurs because the quiescent collector currents of Q_1 and Q_2 are both equal to $\alpha I_{EE}/2$, but $I_{C1} = I_{C3} + I_{B3} + I_{B4}$, so $I_{C4} < I_{C2}$ (quiescent currents) by a small amount. The difference must flow through the load, which results in a non-zero output voltage. Referring to the circuit diagram in the previous problem, show that the input offset voltage related to this effect is given by the expression below, where β_P is the beta value of Q_3 and Q_4. Assume that the circuit is otherwise balanced. *Hints*: 1) If $v_{IN} = 0$ and the offset effect were not present, then $i_{C2} = i_{C4}$, and no current would flow through the parallel combination of r_{o2}, r_{o4}, and R_L, which would yield $v_O = 0$. (In this context, collector currents i_{C2} and i_{C4} are the currents that are generated by the dependent current sources in the hybrid pi model and exclude the currents through r_{o2} and r_{o4}.) 2) Because i_{C2} is not exactly equal to i_{C4}, some current flows through the parallel combination of r_{o2}, r_{o4}, and R_L, even if $v_{IN} = 0$, which creates a non-zero output voltage. 3) Note that $2/\beta_P << 1$.

$$V_{OS} \approx -\frac{2\eta V_T}{\beta_P}$$

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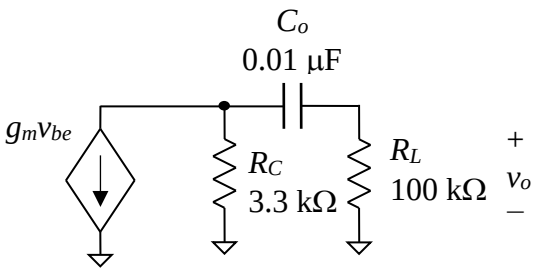
***Ungraded Problems*:**

The following problems will not be graded. However, you should attempt to solve them on your own and then check the solutions. Try not to give up too quickly if you struggle to solve any of them. Move on to a different problem and then come back to the difficult one after a few hours.

1. The diagram below is the small-signal model of the output port of a common-emitter amplifier and its load. Show that the output voltage is given by the symbolic expression shown next to the diagram. Briefly explain the significance of the frequency-dependent part of the expression (the fraction to the right of $R_C \| R_L$).



$$v_o = -g_m v_{be}\left(R_C \| R_L\right)\frac{j\omega\left(R_C + R_L\right)C_o}{1 + j\omega\left(R_C + R_L\right)C_o}$$

2. For the partial amplifier small-signal model considered in the previous problem, find the cut-off frequency (in Hz) associated with capacitor C_o. Then, assuming that $v_{be} = v_{in}$, calculate the magnitude of the midband voltage gain v_o/v_{in} and the magnitude of the voltage gain at the cut-off frequency. Assume that the amplifier has a quiescent current of I_C = 2.0 mA, the emission coefficient is η = 1, and V_T = 25 mV.