Homework Assignment #9 – due via Moodle at 11:59 pm on Friday, April 19, 2024
[Graded Prob. 3 deferred to HW #10]

Instructions, notes, and hints:

You may make reasonable assumptions and approximations to compensate for missing information, if any. Provide the details of all solutions, including important intermediate steps. You will not receive credit if you do not show your work.

Unless otherwise specified, you may assume that all BJTs are at room temperature, the emission coefficient $n = 1$, V_{BE} (or V_{EB} for *pnp* types) = 0.7 V (quiescent value), and $V_{CE}|_{sat}$ (or $V_{EC}|_{sat}$ for *pnp* types) = 0.2 V. If the Early voltage V_A is not specified, you may ignore its effects.

The first set of problems will be graded and the rest will not be graded. Only the graded problems must be submitted by the deadline above. Do not submit the ungraded problems.

Graded Problems:

1. [adapted from Prob. 10.40 of Sedra & Smith, 7th ed.] Consider an ideal voltage amplifier with a voltage gain A_v as shown in the figure below. (The triangle is not meant to represent an op-amp here. A triangle with one input and one output is a standard block diagram symbol for an amplifier.) An ideal voltage amplifier has an infinite input resistance and zero output resistance. As shown in the diagram, a resistor R with a value of 100 kΩ is connected from the output port to the input port of the ideal amplifier so that the overall circuit does not perform ideally. Using the Miller theorem, find the equivalent input resistance R_{in} of the overall amplifier circuit with the feedback resistor present for the following two cases, and comment on the significance of the results.
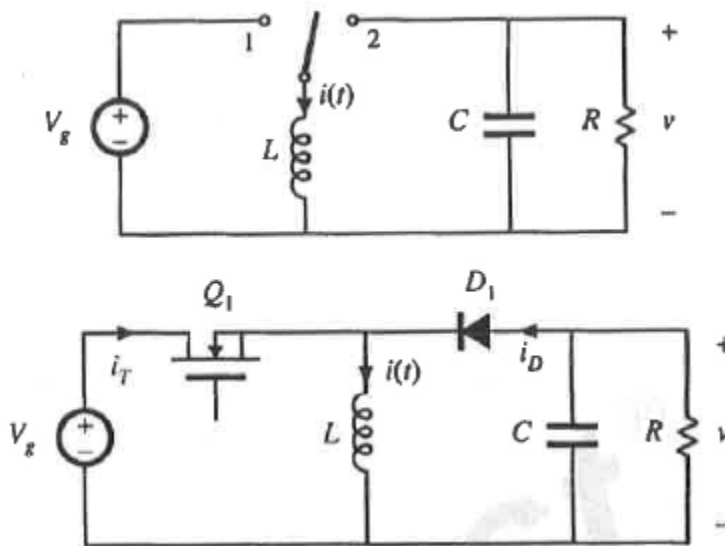
    a. $A_v = -20$ V/V
    b. $A_v = +0.95$ V/V

$R = 100$ kΩ

A_v

v_o

R_{in}
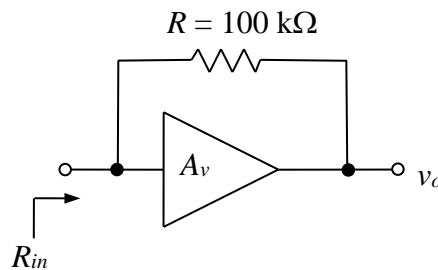
2. [adapted from Prob. 2.1acd of Erickson and Maksimovic, *Fundamentals of Power Electronics*, 2nd ed.] A voltage inverter circuit (called a "buck-boost converter" in Erickson and Maksimovic) is illustrated in the upper diagram below. It is designed to produce a negative output voltage for a positive input voltage (or vice versa). A practical implementation of the circuit using a MOSFET and a diode is shown in the lower diagram. Assume that all components are ideal and that there is no significant voltage drop across the diode. The switch is in position 1 during the DT_s interval of the switching cycle, where D is the duty cycle and T_s is the switching period (the inverse of the switching frequency).

   a. Find the dependence of the equilibrium output voltage V and inductor current I on the duty cycle D, input voltage V_g, and load resistance R. You may assume that the inductor current ripple and capacitor voltage ripple are small. Use the principles of volt-second balance and charge balance to obtain your answers.
   b. If the input voltage is $V_g = 30$ V, the desired output voltage is $V = -20$ V, the anticipated equivalent load resistance is $R = 4\ \Omega$, and the switching frequency is $f_s = 40$ kHz, find D and I.
   c. For the same conditions in part b, calculate the value of L that will make the peak (not peak-to-peak) inductor current ripple Δi equal to ten percent of the average inductor current I. *Hint*: Find an expression for the slope of the inductor current vs. time for either the DT_s or $(1 - D)T_s$ interval of the switching cycle.
   d. For the same conditions in part b, find the value of C necessary to keep the peak output voltage ripple Δv less than 0.1 V. *Hint*: Find an expression for the slope of the capacitor voltage vs. time for either the DT_s or $(1 - D)T_s$ interval of the switching cycle.
   e. Sketch the transistor drain current waveform $i_T(t)$ for your design (parts b, c, and d). Include the effects of inductor current ripple, and indicate the peak value of i_T. Also sketch $i_T(t)$ for the case when L is decreased such that Δi is 50% of I. What happens to the peak value of i_T in this case?

3. **[deferred to HW #10]** [adapted from Prob. 3.1 of Erickson and Maksimovic]: In the voltage inverter circuit (called a "buck-boost converter" in Erickson and Maksimovic) shown below, the inductor has winding resistance R_L. All other losses can be ignored.

   a. Applying the same approximations used in Chap. 3 of Erickson and Maksimovic, derive an expression for the voltage conversion ratio V/V_g that includes the nonzero inductor winding resistance. Ignore the diode voltage drop and the equivalent "on" resistances of the diode and FET. The FET is on (conducting) during the DT_s switching interval.
   b. Derive an expression for the efficiency of the converter circuit. Manipulate your expression into a form similar to Eqn. (3.35) in *Fundamentals of Power Electronics*, 2nd ed.
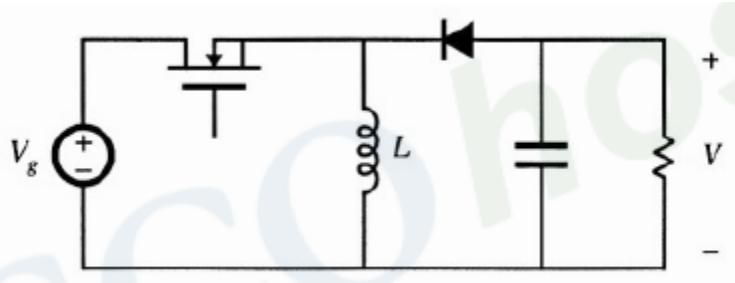

4. In one of the lectures, the relationship shown below right, which is used to determine the value of the inductor L in a boost converter circuit, was derived by setting the time derivative of the inductor current, di_L/dt, equal to the slope of the rising inductor current during the DT_s interval (i.e., during the periods when the pulse-width-modulated switching voltage is high). Show that the same expression for L can also be found by considering the downward slope of the inductor current during the $(1-D)T_s$ interval. Assume that all components in the circuit are ideal and that the ripple on the output voltage is negligibly small.
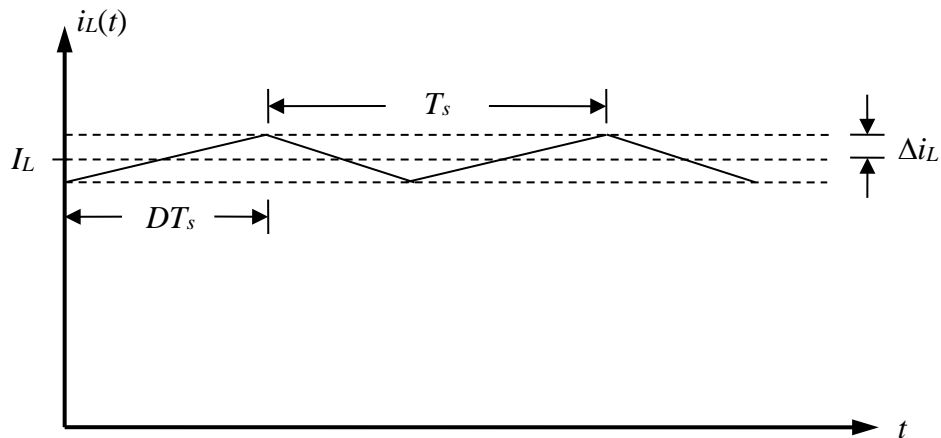

$$L = \frac{V_{IN} DT_s}{2\Delta i_L}$$

5. Shown below is an unusual switching regulator circuit designed to produce a positive or negative output voltage depending on the relative values of positive DC input voltages V_1 and V_2. The switch is implemented using synchronized MOSFETs (not shown). Variable D is the duty cycle, whose value is in the range $0 < D < 1$. As indicated in the conceptual diagram below, the switch is in the lower position during the DT_s time intervals, where T_s is the period of the switching waveform, and in the upper position during the $(1 - D)T_s$ time intervals. Use the inductor volt-second balance principle to find an expression for V_o in terms of the DC voltages V_1 and V_2 and the duty cycle D for the case when $V_1 > V_2$ and the case when $V_2 > V_1$. (Both cases should yield the same expression.) Sketch V_o vs. D for $0 < D < 0.8$ for the $V_1 = 2.0$ V and $V_2 = 4.0$ V case and for the $V_1 = 2.0$ V and $V_2 = 1.0$ V case. (Both curves approach positive or negative infinity for $D \rightarrow 1$.) You may sketch both curves on the same plot. Assume that the inductor current ripple and the capacitor voltage ripple are each small, that the MOSFETs operate like ideal switches, and that the inductor winding resistance can be ignored.
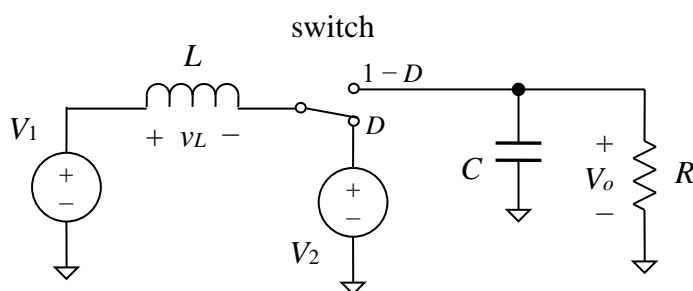
Ungraded Problems:

The following problems will not be graded. However, you should attempt to solve them on your own and then check the solutions. Do not give up too quickly if you struggle to solve any of them. Move on to a different problem and then come back to the difficult one after a few hours.

1. [adapted from Prob. 2.4 of Erickson and Maksimovic]: The switches in the converter shown below operate synchronously; each is in position 1 for $0 < t < DT_s$ and in position 2 for $DT_s < t < T_s$. Assuming that $|V| < V_g$, where V_g is a DC source voltage, derive an expression for the voltage conversion ratio V/V_g, and sketch V/V_g vs. D. The principles of inductor volt-second balance and capacitor ampere-second balance (capacitor charge balance) and the small-ripple approximation may be applied to this problem. The switching frequency is constant, so the output voltage is nearly constant (DC).
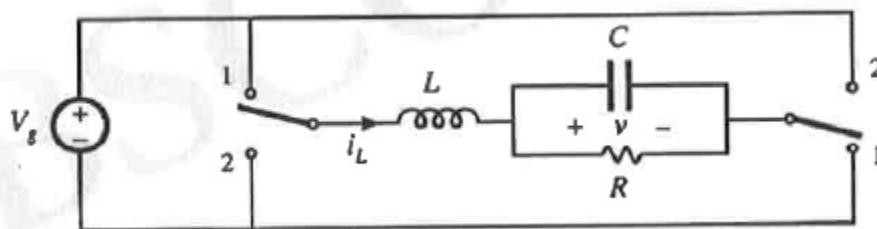
2. The expression for the output voltage V_o of a boost converter for the case of a nonzero inductor wire resistance R_w is given below. The other variables in the expression are D = duty cycle and R_L = equivalent load resistance. Suppose that the input voltage V_{in} is being supplied by a battery with a nonzero internal resistance R_{int}. That is, the battery is represented by a Thévenin equivalent circuit consisting of voltage source V_{in} in series with resistance R_{int}. Explain how the internal resistance would be incorporated into the expression below; that is, explain how the expression should be modified. Which resistance (R_{int} or R_w) is likely to be the dominant factor that limits the output voltage?

$$V_o = \frac{V_{in}}{1-D} \cdot \frac{1}{1 + \dfrac{R_w}{(1-D)^2 R_L}}$$

3. The amplifier shown below was analyzed in Ungraded Prob. 3 of HW #7. The amplifier has a quiescent collector current of around 500 μA, a midband gain of −180 V/V, an upper cut-off frequency of approximately 3.4 MHz, and an input resistance of approximately 500 Ω. The input resistance is much lower than that found for common-emitter amplifiers with the more conventional emitter degeneration biasing method (i.e., using R_E). The reduction is caused by the feedback introduced by resistor R_1. Use Miller's theorem to confirm the estimate of the midband input resistance R_{in} seen by the signal source. The value that you obtain might not agree exactly with the one found earlier. Remember that that value and the one obtained via Miller's theorem are *estimates*.
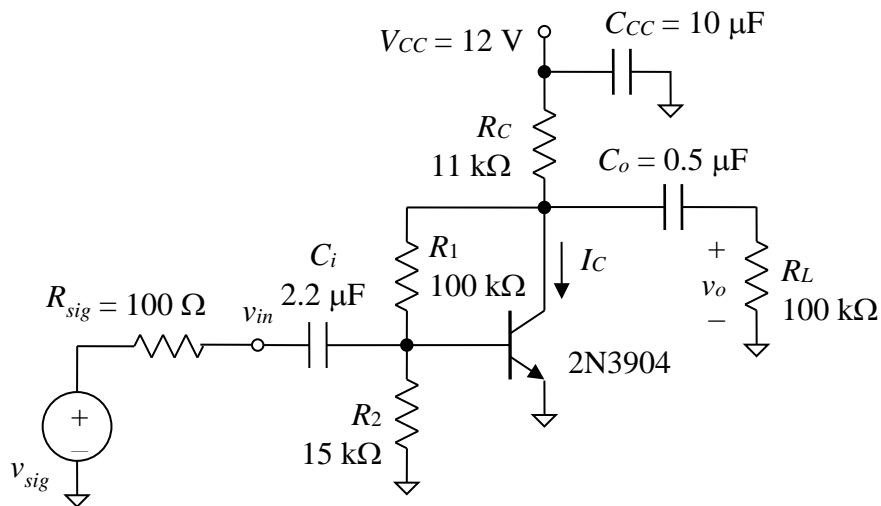
4. For the amplifier in the previous problem, use Miller's theorem to confirm the estimate of the upper cut-off frequency f_H of the amplifier due to the combined effects of BJT capacitances C_π and C_μ. Remember that the effect of C_μ is modeled by adding a new capacitance across the input port and another one across the output port. As with the input resistance in the previous problem, the value for f_H that you obtain here might not agree exactly with the one found earlier because both are estimates.