Lab #4: Amplifier with Specified Frequency Response

Introduction

The focus of this lab exercise is to design and build a common-emitter amplifier with a specified lower cut-off frequency and with an upper cut-off frequency determined by the limits of the BJT used. You will also encounter a potential source of measurement error and learn the importance of using appropriate measurement tools for demanding tasks. Furthermore, you will have an opportunity to assemble the amplifier circuit on a printed circuit board fabricated using modern methods, which should give you an appreciation of some of the challenges of prototyping. Randomly assigned lab groups are listed at the end of this handout.

Theoretical Background

Figure 1 depicts the usual common-emitter amplifier circuit topology. The BJT type and power supply voltage are specified so that there is some consistency between lab groups. The load is modeled as a resistance R_L in parallel with a capacitance C_L. The latter element could represent the capacitance between a circuit board trace and the ground plane of a printed circuit board, the input capacitance of a following amplifier stage, or the capacitance of an interconnecting cable such as a coaxial cable. In this lab exercise, it primarily represents the capacitance of the test leads connected to the oscilloscope. The load resistance R_L could represent a transducer of some kind (like an ear bud or speaker), the input resistance of a following amplifier, the equivalent input resistance of a test instrument (like an oscilloscope), or a combination of two or more of these loads. In this lab exercise the load will consist primarily of the oscilloscope.

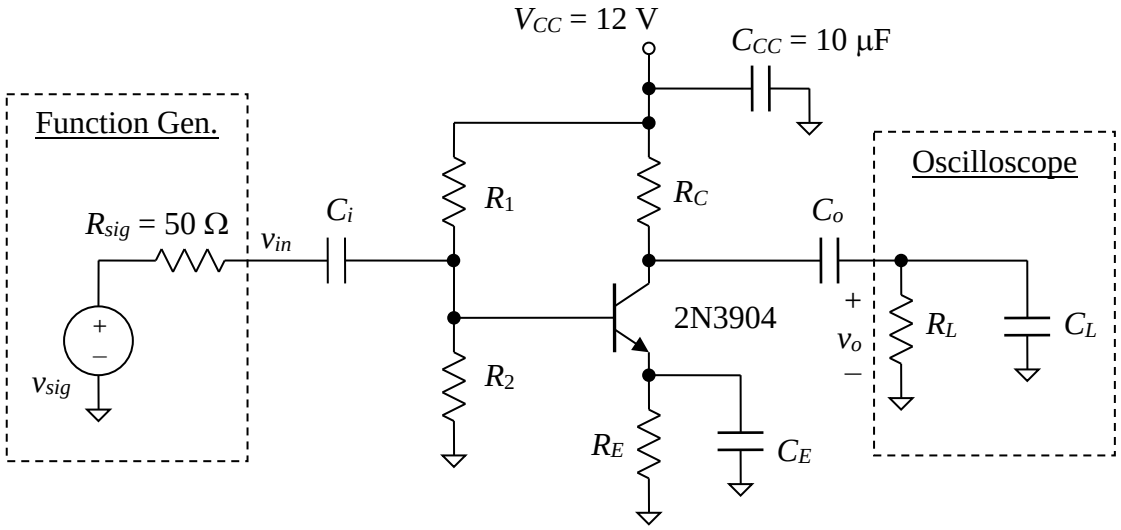

Figure 1. Common-emitter amplifier with capacitive load. The components R_L and C_L model the combination of the input port of a following circuit stage and a test probe. The elements surrounded by dashed lines and labeled “Function Gen.” and “Oscilloscope” are not part of the amplifier circuit and are not mounted on the printed circuit board.

Experimental Procedure

- Design a common-emitter amplifier like the one shown in Figure 1 to meet the following specifications:

  BJT type: 2N3904
  Power supply voltage: 12 VDC (unipolar)
  Small-signal midband voltage gain magnitude (with > ~100 kΩ load): ~180 V/V
  Lower limit of operational frequency range: 300 Hz
  Keep the total low-frequency capacitance ($C_i + C_o + C_E$) as small as possible, assuming that R_L = 1.0 MΩ.
  Upper limit of operational frequency range: whatever the BJT allows
  Maximum midband output voltage swing above and below quiescent: ±1 V
  Minimum midband input resistance for all possible values of β: 2 kΩ

  The signal source is the function generator, which has an output impedance of 50 Ω.

  Important Design Information:

  - The input impedance of the oscilloscopes in our labs is modeled as 1 MΩ of resistance in parallel with 14 pF of capacitance. Those values are usually printed next to the oscilloscope's jacks corresponding to each channel. The equivalent input impedance of the oscilloscope's port is in parallel with the amplifier's load. A test cable can add considerable capacitance in parallel with the equivalent port impedance; the cable capacitance is added to the 14 pF of jack capacitance. The simple cables with alligator clip leads used in the Bucknell labs each have about three feet of RG-58A/U coaxial cable, which adds about 90 pF of capacitance. You can verify this by consulting the information on coaxial cable characteristics available via the link provided on the Laboratory page at the course web site ("RF Café – Coaxial Cable Characteristics"). High-quality "×10" test probes have a significantly different model associated with them that you will need to obtain at some point. That type of probe usually has a combined model that accounts for both the cable and the input jack of the oscilloscope.

  - The quiescent collector current is not specified, nor are there any other restrictions on the bias circuit design. It is up to you to select reasonable component values that satisfy the specifications yet do not exceed the various device ratings and other practical limits. *Hint*: The quiescent voltage across R_C in this circuit is directly related to a good approximate expression for the small-signal voltage gain. You might want to derive the relationship before you proceed with your design. You will probably not be able to divide V_{CC} equally between R_C, V_{CE}, and R_E; that is, the $V_{CC}/3$ rule-of-thumb might not work.

  - To suppress noise and prevent oscillations, remember to include bypass capacitor C_{CC} between the power supply lead and ground (10 μF recommended). Keep these connections relatively short, and pay attention to the capacitor's polarity. You might want to consider placing an additional capacitor with a value of 0.1 μF or so in parallel with the larger bypass capacitor. There should be room for it on the circuit board that will be provided to you. Parallel capacitors with widely varying values are often used to mitigate problems with power supply noise and/or feedback over wide frequency ranges.

- Pay close attention to the maximum ratings on the 2N3904 data sheet, such as the maximum power dissipation and the maximum collector-emitter voltage. Also pay attention to resistor power ratings, capacitor voltage ratings, and capacitor polarity.

- It is not necessary to account for the capacitance of the cable between the signal source and the input port of the amplifier nor that of the input test leads. Both capacitances can be treated as part of the TEC of the signal source. The value of R_{sig} is so small that the capacitive reactance of the input cables is negligible at the frequencies that we are considering because the associated pole frequency is so high. Also, the amplifier's input voltage v_{in} is measured at the amplifier side of the cable, so the input cable capacitance does not affect the gain (v_o/v_{in}) anyway.

- Keep a detailed record of the design choices that you make. Be able to explain your choices for the values of all resistors and capacitors. You will be required to provide a brief summary of your frequency response analysis at the end of the lab exercise.

- You may build an early prototype of the amplifier on a protoboard for partial testing and/or you may simulate the circuit using the *Multisim* software package. Note, however, that the circuit could become unstable if it is assembled on a protoboard.

The following bullet (with notes) should be completed before the second lab session.

- Assemble the amplifier using one of the available printed circuit boards. Timely assembly of your circuit board will be a factor in your overall lab score. Pay close attention to the guidelines below. **Your lab score will be reduced if you must assemble a new circuit on a second printed circuit board for a reason related to the notes below.**

  Important Assembly Notes:

  - You may mount the components on either the trace side or the ground plane side of the printed circuit board (PCB). To allow access to the leads with the soldering iron and to avoid melting parts, **solder the leads on the side of the PCB where they protrude.** Be very careful when you install the 2N3904 and the polarized capacitors. Double-check their orientations before soldering.

  - Remember that v_{sig}, R_{sig}, R_L, and C_L are not physical components mounted on the PC board. They represent the function generator and the oscilloscope.

  - The power supply leads should be made from roughly one-meter lengths of #20 or #22 insulated wire (available in the Maker-E). Consider twisting the leads to minimize noise pick-up and wire tangles. Tin (apply solder to) the ends of the power leads that will be connected to the power supply. Tinning helps prevent corrosion and fraying of the stranded copper filaments that make up the wire.

  - To allow connections to be made to the test equipment, solder test points into the appropriate places on the PC board, one for the probe hook and one for the ground clip. Test points will be provided to you. Make sure that there is sufficient clearance around the test points for the oscilloscope leads so that they do not touch each other, circuit components, or the ground plane (unless they are supposed to be grounded, of course).

- Apply DC power (but not yet a signal) to the assembled amplifier, and verify by measurement that the quiescent voltages are reasonably close to their design values.

- Use the function generator and oscilloscope to verify that the amplifier is achieving the target midband gain and **lower** cut-off (−3 dB) frequency. **Do not** use the high-quality (×10) test leads to connect the function generator to the input of the amplifier; they are not designed for that purpose. If necessary, add an attenuator to the output of the function generator to obtain a sufficiently low input amplitude to prevent clipping and/or nonlinearity. For this test, you may use the low-quality test leads with alligator clips for the connections to the oscilloscope.

- Identify and correct any wiring, soldering, and/or component value errors.

- (Measurement) Use the low-quality test leads (the ones with alligator-clips) to connect the output of the amplifier to the oscilloscope. Use either the high-quality (×10) or low-quality leads to simultaneously measure the input voltage. Vary the function generator's frequency over a wide enough range to determine the **upper** cut-off (−3 dB) frequency of the amplifier.

- (Analysis) For the low-quality test leads, use circuit analysis to determine whether the dominant high-frequency pole is due to the total load capacitance C_L (leads plus oscilloscope) or one of the internal BJT capacitances C_π or C_μ. You do not have to consider the internal capacitance between the collector and the emitter since it is not likely to have a significant effect in this type of amplifier because the load capacitance C_L is likely to be much larger in value. Use the information on the 2N3904 datasheet to estimate the values of C_π and C_μ. Capacitance C_μ is often called C_{obo} on datasheets. Capacitance C_π can be determined using the method described in the textbook and in the lecture sessions. Keep good records of your analysis, including the evaluation of the equivalent resistances seen by each capacitance, and your final numerical results. Estimate the upper cut-off frequency f_H from your analysis, and compare it to the measured value.

- (Analysis) Repeat the previous analysis for the high-quality (×10) Agilent 10073D test leads used to measure the output voltage. The primary difference between these leads and the low-quality leads is the equivalent impedance that models the combination of the leads and the oscilloscope input port. The user guide for the probes is available on the Laboratory page at the course web site. (Agilent was renamed Keysight many years ago.) Note that the input of the Agilent 10073D probe can be modeled as a resistance of 2.2 MΩ in parallel with a capacitance of 12 pF. As with the low-quality leads, record a detailed summary of your analysis and your final numerical results. Estimate the upper cut-off frequency f_H from your analysis.

- (Measurement) Now use a high-quality (×10) probe to connect the output of the amplifier to the oscilloscope, and, if possible, determine the upper cut-off frequency. The new cut-off frequency might be above the upper frequency limit of the function generator. If that is the case, try to estimate the cut-off frequency by noting the decrease in gain vs. frequency as the frequency is increased. Compare your measured value of f_H to the analytical value that you found in the previous bullet.

- Capture an oscilloscope screen image of the input and output voltage waveforms being simultaneously displayed. Choose a frequency in the midband region, and adjust the image so that it clearly demonstrates the target midband voltage gain. Follow the guidelines available at the Laboratory web page to prepare a professional-quality document containing the screen image and a thoroughly descriptive caption that includes a comparison of the measured gain to the designed gain. (Start the caption with the text "Figure 1.") Make sure that relevant items such as the frequency of operation and trace identification are included in the caption. The screen image must be submitted before the post-lab meeting (see next bullet).

- For fun, increase the magnitude of the sinusoidal input voltage, and observe the oscilloscope traces of the input and output voltage waveforms. You should see significant distortion begin to appear as the input signal increases. Try to explain why the amplifier clips at the observed voltage levels. This activity is for your own edification. You do not have to submit evidence that you observed simulated distortion.

- Compile the following material for reference during the post-lab meeting. All items should be legible and well organized. Figures, tables, captions, and equations must be formatted according to the guidelines posted on the Laboratory page at the course web site.Add your names, the lab number (Lab #4), the course number (ECEG 351), and the semester (Spring 2024) to all submitted items.

    - Diagram of the amplifier circuit with component values and key voltages and currents clearly indicated
    - Brief outline of the design process, especially the determination of equivalent resistance values and the selection of capacitor values to set the value of f_L
    - Quiescent collector and emitter voltage measurements
    - Determination of f_H for low-quality (alligator-clip) test leads using circuit analysis and comparison to measured value
    - Determination of f_H for high-quality (×10) test leads using circuit analysis and comparison to measured value
    - Properly labeled, annotated, and captioned oscilloscope screen captures of input/output voltage waveforms showing linear operation in the midband range and that the specified midband gain has been achieved

    Combine all of the items above into a single PDF document and **e-mail** it to me before the post-lab meeting begins. The file name format should have the form:

    "LName1_LName2_LName3_Lab4_sp24.pdf"

    Add "LName4" if your group has four members. **The file size must be less than 5 MB.** Keep a copy if you wish to use it to prepare for the next exam or need it for future reference.

- Schedule a post-lab meeting (length up to 30 min) with me at a mutually agreed time before the deadline posted on the Laboratory page at the course web site. The purpose is to assess each group member's comprehension of the design process, measurements, and observations of circuit performance. The meeting could cover any aspect of the design and related topics. The following guidelines apply:

- Read these guidelines and the "Post-Lab Meeting" section below well in advance of the meeting.
- All group members must be present.
- The meeting will take place in the Maker-E if Dana 307 is not available at the scheduled time.
- Meetings will be scheduled in the order that requests are received. The order might be determined by random assignment. Meetings will not be scheduled during a lecture, lab, or recitation section for another course. Please notify me of time conflicts.
- Meetings will not be rescheduled if the first one reveals circuit problems, wiring failures, errors in the test procedure, or a lack of preparation.
- Deadline extensions will generally be approved for confirmed illnesses or other extenuating circumstances.
- Meetings may take place before the end of a lab session if other groups do not need assistance. You do not have to remain in the lab room after the meeting ends.

Post-Lab Meeting

At the beginning of the meeting, your group must verify by measurement that the quiescent collector and emitter voltages are close to the chosen design values. Afterward, each group member will be asked to respond to one of the prompts from the numbered list starting below and possibly answer a few follow-up questions. The following guidelines apply:

- Each person will have a time limit of **five minutes** in which to respond.
- You may assign the prompts to group members before the meeting.
- Each response must be supported by high-quality visual aids prepared by the respondent, including a properly labeled circuit diagram (or diagrams).
- The physical circuit layout and connections to equipment should be organized so that group members can switch between demonstrations quickly.
- Visual aids must be complete enough for understanding but not so information-packed that they are overwhelming or create visual clutter that detracts from clarity.
- Figures, tables, captions, and equations must be formatted according to the guidelines posted on the Laboratory page at the course web site.

The four prompts are listed below:

1. Explain how your group selected appropriate resistor values to achieve the specified midband gain and ±1 V output voltage swing while simultaneously ensuring a stable bias point. Verify the midband gain by measurement.
2. Explain how you determined the capacitor values required to achieve the specified lower cut-off frequency f_L while minimizing the total required capacitance. You do not have to show how the equivalent resistances seen by the capacitors were determined, but you should show the formulas that you used/derived. Verify the value of f_L by measurement.
3. Explain the analysis procedure used to determine the upper cut-off frequencies f_H when high-quality and low-quality test leads were used to connect the output of the amplifier to the oscilloscope. Verify the calculated values of f_H by measurement to the extent possible.
4. **[for 4-person groups only:]** Explain how your group ensured during the design process that the midband input resistance of the amplifier was at least 2 kΩ.

Lab Scoring Criteria

Each group member will receive a score based on the following criteria quantized at the indicated levels. The first three criteria constitute a group base score; that is, each group member will receive the same score for those criteria. The remaining criteria will be assessed independently and will be determined by that person's contribution to the post-lab meeting. The rubric posted on the Laboratory page at the course web site will guide the assignment of scores.

0, 10, 15, 20 pts	Properly assembled amplifier (group)
0, 8, 15, 23, 30 pts	Functional amplifier that meets specifications (group)
0, 2, 5, 8, 10 pts	Properly labeled, annotated, and captioned screen capture (group)
0, 2, 5, 8, 10 pts	Quality and effectiveness of supporting visual aids (indiv.)
0, 8, 15, 23, 30 pts	Quality of response to prompt (indiv.)
−5 pts/extra board	Use of two or more printed circuit boards

If the meeting is completed after the deadline, a 10% score deduction will be applied for every 24 hours or portion thereof that it is late (not including weekend days) unless extenuating circumstances apply. No credit for the individual criteria will be given four or more days after the deadline; however, up to 60 pts will be assigned to each member of the group for the group criteria if at least one group member demonstrates an assembled and functional amplifier within a week of the deadline.

Group Assignments

The randomly generated groups for this lab exercise are listed below:

Andrews-Ren-Sagoe
Piper-Powick-Tuncel
Beebe-Jiorle-Samuels-Youn