Lab #5: A Simple Boost Converter

Introduction

The focus of this lab exercise is to build a boost converter circuit designed to take a 3.0 V DC input and produce a 6.0 V DC output. Your primary tasks will be to observe the nonideal properties of the circuit, attempt to mitigate some of the nonideal behavior, and observe some of the factors that impose practical limits on the output voltage and efficiency of actual boost converter circuits. Lab group assignments are listed at the end of this handout.

Theoretical Background

A basic boost converter circuit is depicted in Figure 1. The MOSFET operates as a switch and alternates between operation in the cut-off region (when V_{PWM} is "low," or at 0 V) and the triode region (when V_{PWM} is "high," or at a positive voltage greater than the threshold voltage V_t of the MOSFET). To gain an approximate sense of how the circuit works, it is typically assumed that the drain-source path of the MOSFET has a resistance close to zero when the MOSFET is in the "on" state and infinity in the "off" state. The load is modeled as a resistance R_L; it represents the actual device to be powered that is connected to the output of the converter. Ideally, the output voltage v_O should stay nearly constant regardless of the load, but the output current i_O varies depending on the power demand. Thus, the equivalent load resistance R_L can vary from a minimum value of $v_O/i_{O\,\max}$ to a maximum of infinity (for $i_O = 0$). A Schottky diode is used in the circuit because it has a lower turn-on voltage than a standard *pn* junction diode. The design of boost converters is detailed in Chapter 2 of [1], and some of the nonideal aspects of their operation, such as the effects of inductor winding resistance, are detailed in Chapter 3 of [1].

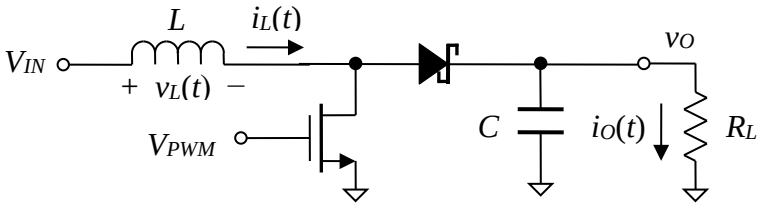

Figure 1. Basic boost converter circuit. Voltage V_{PWM} is a pulse width-modulated rectangular wave with duty cycle D, where $0 < D < 1$. The duty cycle is the ratio of the "on" time per period to the duration of the total period T_s.

The pulse width-modulated voltage V_{PWM} can be generated by any clock circuit with a variable duty cycle. In practice, the duty cycle is controlled automatically by a feedback circuit. However, in the interest of simplicity and to save time, in this lab exercise we will use the bench-top function generator to supply the PWM signal. The duty cycle can be controlled manually between 20% and 80%. (See the function generator manual available on the Laboratory page at the course web site.)

Experimental Procedure

- Assemble a boost converter like the one shown in Figure 1 to meet the following specifications:

  MOSFET type: 2N7000 or BS170
  Diode type: SB130 Schottky
  PWM control signal pulse rate f_s: 75 kHz
  Approx. input voltage V_{IN}: 3.0 VDC
  Average output voltage V_O: 6.0 VDC
  Maximum output current: 5.0 mA (equivalent load resistance is 6/0.005 = 1.2 kΩ)
  Peak (not pp) output voltage ripple Δv_o: 10 mV
  Peak (not pp) inductor current ripple Δi_L: 1.0 mA

  Based on the specifications, the duty cycle D, the inductor value L, and the capacitor value C should be (using formulas found in [1])

$$V_O = \frac{V_{IN}}{1-D} \quad \rightarrow \quad D = 1 - \frac{V_{IN}}{V_O} = 1 - \frac{3}{6} = 0.5\,,$$

$$L = \frac{V_{IN} D}{2\Delta i_L f_s} = \frac{(3.0)(0.5)}{2(0.001)(75\text{k})} = 10 \text{ mH},$$

  and

$$C_{\min} = \frac{D}{2(\Delta v_o / V_O) R_{L\min} f_s} = \frac{0.5}{2(0.010/6.0)(1,200)(75\text{k})} = 1.7\ \mu\text{F}.$$

  Pay close attention to the maximum ratings for all components, such as maximum power dissipation and maximum allowable voltages and currents. Double-check the orientations of the MOSFET, the diode, and all electrolytic capacitors before applying power.

- Use the bench-top function generator to drive the switch transistor. For instructions on adjusting the duty cycle, consult the manual available at the course web site.

- Keep complete and well-organized records in case you must make changes and/or for reference during the lab summary meeting. At a minimum, you should record any changes that you make to component values and/or the duty cycle.

- Apply power to the circuit, and observe the output voltage waveform at full rated output current (i.e., with a 1.2 kΩ test resistor serving as the load). Check for component overheating and that the output voltage is nominally correct with a ripple that is within specifications. Adjust the duty cycle of the PWM waveform if necessary; if you do, record the value at which you obtain acceptable performance. You will probably observe several unusual or unexpected features in the output waveform such as voltage spikes. There are many possible causes for the various nonideal characteristics, including charging and discharging of the MOSFET and diode internal capacitances and the presence of stray inductances. Try some or all of the following potential remedies, and record their effectiveness:

- Shorten long, looping wires, and reduce the spacing between components on the protoboard.
- Form the long leads from the power supply to the protoboard into a twisted pair.
- Add a resistor in series with the gate of the MOSFET. Adjust the value and determine the order of magnitude that seems to be the most effective. Try a few hundred ohms, a few thousand, and perhaps values in the tens or hundreds of kilohms.
- Add a resistor (large value!) in parallel with the diode. Adjust the value and determine the order of magnitude that seems to be the most effective. If it does not improve the performance very much or at all, try adding a capacitor in parallel instead, and adjust its value. Start with values of a few or tens of nanofarads.
- Try other potential remedies. Experiment! Record anything that is effective.

- **Make sure that your circuit is working properly and reliably BEFORE the second lab session.** After you are confident that your circuit is meeting all specifications, at least partially (and you have a reasonable explanation for partial performance), and that you have taken all possible steps to reduce or eliminate the undesirable features of the output waveform, capture an oscilloscope screen image of the waveform with the ripple clearly visible while the converter is supplying the maximum rated current to the load at the specified output voltage. Record the relevant conditions under which the measurements were performed and descriptions of any noteworthy features of the image.

- Increase the output voltage above 6.0 V by changing the duty cycle. In theory, you should be able to raise the voltage to several times the input level of 3.0 V, but you should find in practice that the maximum output voltage is severely limited. Make sure that you understand why. You should carefully read Sections 3.2 and 3.5 in Erickson and Maksimovic [1]. Measure and record the DC resistance of the inductor, and record your observations. The maximum and minimum duty cycles of the function generators are 80% and 20%, respectively, so your ability to change the output voltage will be somewhat constrained.

- Return the duty cycle to the value that produces V_O = 6.0 V. Increase the load resistance to a value a little beyond the point where the converter enters discontinuous conduction mode (DCM) and observe what happens. You may use a potentiometer for the load resistance to make this adjustment easier. Predict the output current level at which the transition should occur, and compare your prediction to your observation. Be prepared to explain how to tell when the transition from continuous conduction mode (CCM) to DCM takes place.

- Compile the following material for reference during the lab summary meeting, **which will take place during the second lab session on April 25**. All items must be legible and well organized. Figures, tables, captions, and equations must be formatted according to the guidelines posted on the Laboratory page at the course web site. Add your names, the lab number (#5), the course number (ECEG 351), and the semester (Spring 2024) to all submitted items. The quality of the submitted material will affect your overall Lab #5 score.

    - Diagram of the converter circuit with all component values or types clearly indicated. Be sure to include any new ones that were added to mitigate nonideal performance.
    - Any graphics and/or text required to support your responses to the prompts listed in the next section.

Combine the items above into a single PDF document and **e-mail** it to me before the deadline listed on the Laboratory page at the course web site. (You may e-mail it after the summary meeting.) The file name format should have the form

LName1_LName2_LName3_Lab5_sp24.pdf

Add "LName4" if your group has four members. **The file size must be less than 5 MB.** Keep a copy if you wish to use it to prepare for the final exam or need it for future reference.

Laboratory Summary Meeting

Your lab group will meet with me during a randomly assigned 20-minute time slot during the April 25 lab session. The first 50 minutes of the session will be used for preparation and last-minute troubleshooting. The first meeting will begin at 8:50 am. The following guidelines apply:

- Meeting times will be randomly assigned at the beginning of the second lab session on April 25.
- All group members must be present.
- Meetings will not be rescheduled if the first one reveals circuit problems, wiring failures, errors in the test procedure, or a lack of preparation. Groups that are not prepared to meet during the April 25 lab session and must meet later will be subject to a score reduction as explained in the "Lab Scoring Criteria" section below.
- You do not have to remain in the lab room after your group's meeting ends.
- Deadline extensions will generally be approved for confirmed illnesses or other extenuating circumstances.
- Meetings that must be scheduled after the second lab session will take place in the Maker-E if Dana 307 is not available at the scheduled time.

During the meeting, each group member will be asked to respond to one of the prompts from the numbered list below and possibly answer a few follow-up questions. The following guidelines apply:

- Each person will have a time limit of **five minutes** in which to respond. There will not be time for me to provide hints or to wait for you to formulate an answer, so be prepared for the meeting and thoroughly understand the concept behind your chosen prompt. Think of this as part of your homework for the week.
- Your group may assign the prompts to members before the meeting.
- Each response must be supported by high-quality visual aids prepared by the respondent, including a properly labeled circuit diagram (or diagrams).
- Visual aids must be complete enough for understanding but not so information-dense that they are overwhelming or create visual clutter that detracts from clarity.
- Figures, tables, captions, and equations must be formatted according to the guidelines posted on the Laboratory page at the course web site.
- Your response must demonstrate that you have gained a good understanding of the relevant concept and that you have engaged in some reflection and/or study beyond the basic lab handout and guidance from me.
- The physical circuit layout and connections to equipment should be organized so that group members can switch between demonstrations quickly.

The four prompts are listed below:

1. Display the output waveform, and explain the steps that were taken to eliminate or reduce any undesirable features. Provide sound explanations for their (non)effectiveness.
2. Raise the output voltage by adjusting the duty cycle, and explain why the output voltage is limited. Relate the explanation to the DC resistance of the inductor. The explanation should be at least partially quantitative and related to the assigned reading.
3. Demonstrate the transition from continuous conduction mode (CCM) to discontinuous conduction mode (DCM), and explain how to confirm that the transition takes place.
4. [for 4-person group only] Explain how you confirmed that all circuit components, including the test load but excluding the inductor, operated within their maximum voltage, current, or power ratings, accounting for the duty cycle. The inductor is excluded because a datasheet for it is not available.

Reference

[1] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed., Springer, 2001.

Lab Scoring Criteria

Each group member will receive a score based on the following criteria quantized at the indicated levels. The first three criteria constitute a group base score; that is, each group member will receive the same score for those criteria. The remaining criteria will be assessed independently and will be determined by that person's contribution to the post-lab meeting. The rubrics posted on the Laboratory page at the course web site will guide the assignment of scores.

0, 20, 30, 40, 45, 50 pts	Demonstration of properly operating circuit (group)
0, 2, 5, 8, 10 pts	Fully labeled schematic diagram of amplifier circuit (group)
0, 2, 5, 8, 10 pts	Quality and effectiveness of supporting visual aids (indiv.)
0, 8, 15, 23, 30 pts	Quality of response to prompt (indiv.)

If the lab summary meeting is completed after the posted deadline, a 10% score reduction will be applied for every 24 hours or portion thereof that it is late (not including weekend days) unless extenuating circumstances apply. No credit for the individual criteria will be given if the group does not complete the meeting before the semester ends; however, up to 60 pts will be assigned to each member for the group criteria if at least one group member demonstrates an assembled and functional circuit before the semester ends. If no meeting takes place, then a score of up to 30 points will be assigned to reflect participation during the lab session.

Group Assignments

The randomly generated groups for this lab exercise are listed below:

Beebe-Samuels-Youn
Piper-Ren-Sagoe
Andrews-Jiorle-Powick-Tuncel