Sequential Logic and Flip-Flops

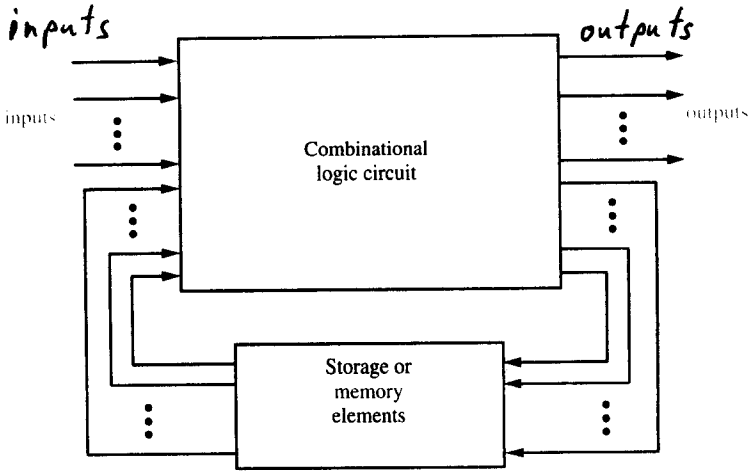
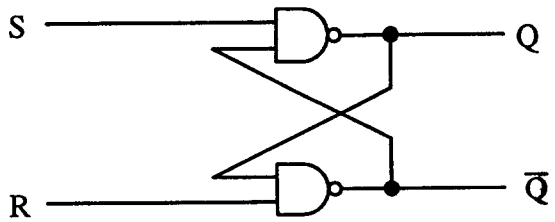


Fig. 12.34 General sequential-logic circuit.

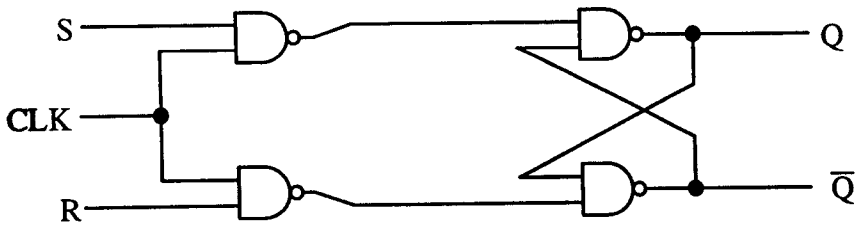
A clock is (usually) included so outputs are computed at discrete times.

SR Flip-Flop:



Present Inputs		Present output	Next output	
$S(t)$	$R(t)$	$Q(t)$	$Q(t+1)$	$\bar{Q}(t+1)$
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Clocked SR:



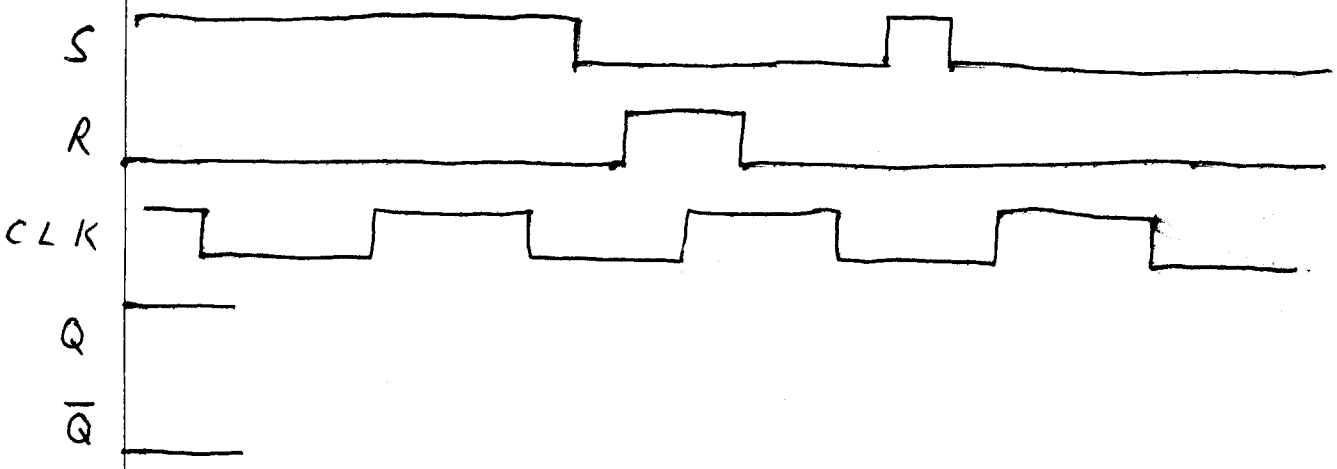
- Truth table
- How to add asynchronous PRESET and CLEAR ?

Interesting case for clocked SR FF:

$S = R = 1$, $CLK = 1 \Rightarrow Q = \_\_\_ \quad \bar{Q} = \_\_\_$

What happens when $CLK = 0$ with $S = R = 1$?

Timing Diagram:



We use clocked SR FF to build other FFs (D, JK)

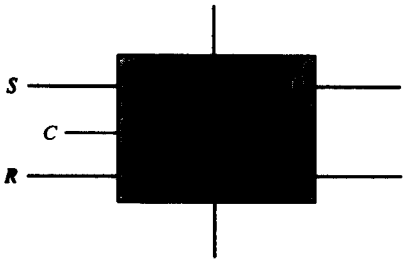


Fig. 12.39 An SR flip-flop with clear and preset inputs.

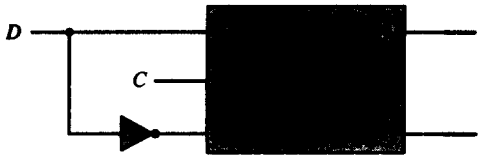


Fig. 12.40 A D flip-flop.

Fig. 12.41 Circuit symbol of a D flip-flop.

Timing for D FF:

"Level triggered" (not "edge triggered")