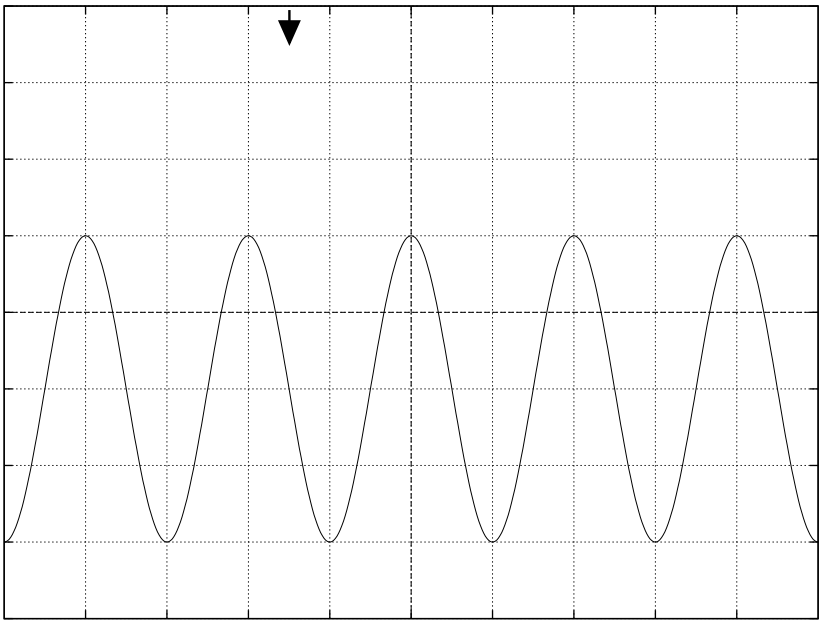
PHYS 235: Homework Problems

1. The illustration is a facsimile of an oscilloscope screen like the ones you use in lab. A sinusoidal signal from your function generator is the input for Channel 1, and your scope is set so that the horizontal axis in the middle of the screen is ground (0 V).



CH1 20.0 mV 500 μs

   (a) What is the Trigger Slope setting: Rising or Falling?

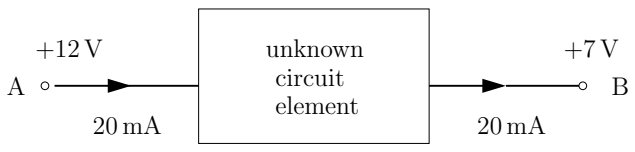
   (b) What is the Trigger Level setting? (This is the voltage value that would be displayed in the lower righthand corner of the screen.)

   (c) Is the CH 1 Coupling set to DC or AC?

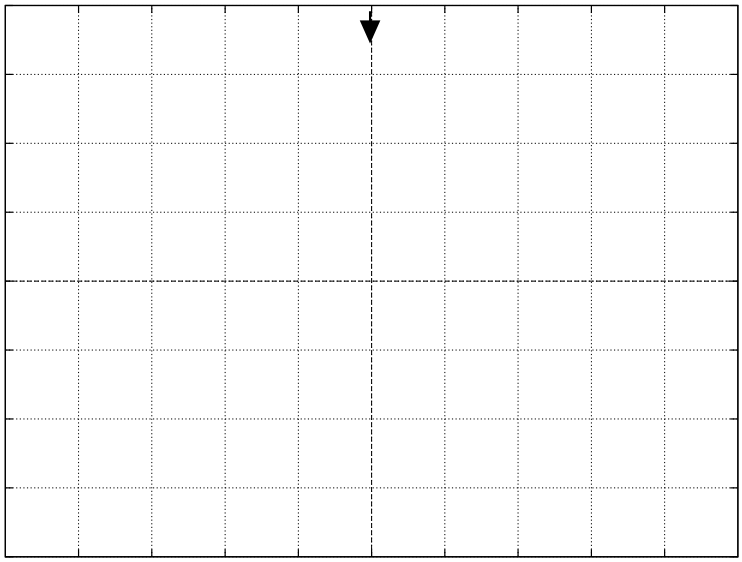
   (d) Using the trigger point as time $t = 0$, determine the function describing the input signal, i.e., determine the constants a, b, c, and d in the expression

$$v(t) = a \sin(bt + c) + d.$$

2. Calculate the resistance between terminals A and B.



3. Your function generator is set to produce a sinusoidal voltage with an amplitude of 0.2 V, a frequency of 100 kHZ, and zero offset. The trigger on your scope is set to `Slope: Rising`, and the trigger level −0.1 V. Sketch the waveform that appears on your oscilloscope. You must indicate horizontal and vertical scale settings on your diagram, and these must correspond to real scale settings on your oscilloscopes. Note that the trigger point is indicated in the illustration, and assume that your scope is set so that the horizontal axis in the middle of the screen is ground (0 V).



4. (a) Define current.

   (b) Define electric potential or voltage. What are the MKS units of potential difference? What does "ground" mean?

5. Consider a copper wire that is 0.25 m long, with a diameter of 0.5 mm. The wire carries a current of 10 mA.

   (a) Calculate the resistance of the wire.

   (b) How many electrons per second flow past a fixed point in the wire?

   (c) What is the voltage drop between the ends of the wire when the 10 mA current is flowing. Is this consistent with the standard approximation that wires are essentially equipotentials?

   (d) What is the drift velocity of the electrons in the wire?

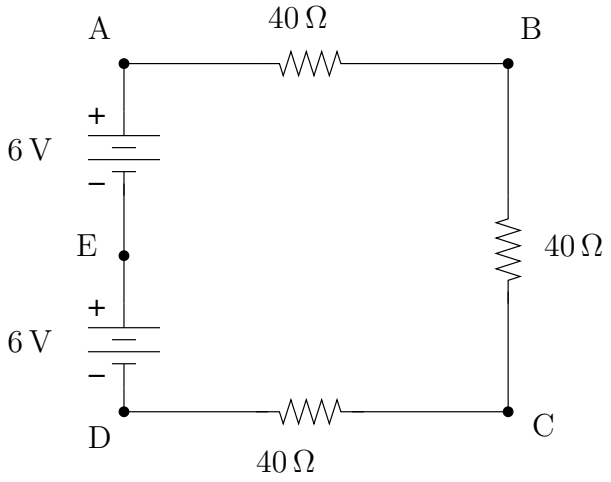
6. Calculate the voltage at points A, B, C, D, and E (relative to ground) if

   (a) point D is grounded,

   (b) point E is grounded,

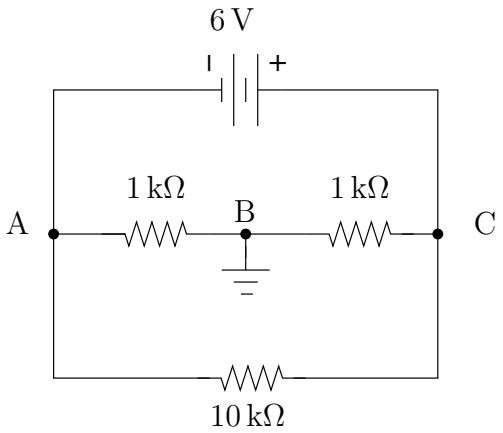
   (c) point A is grounded, and

   (d) point B is grounded.

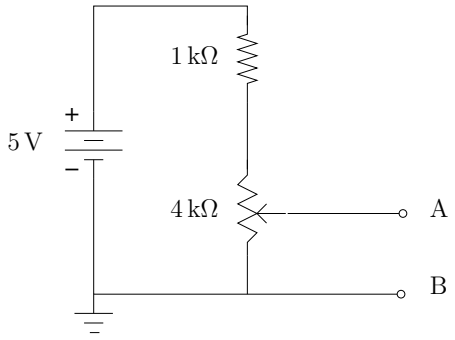


7. The BK Precision power supply on your benchtop has three outputs, labeled `+`, `-`, and `GND`. How should you connect these to get $-5\,\mathrm{V}$ (with respect to ground) to a point on your proto-board?

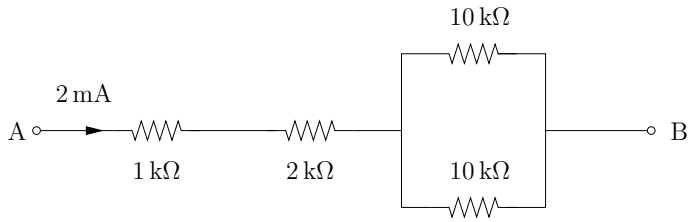
8. Calculate the voltage at points A, B, and C in the illustrated circuit.



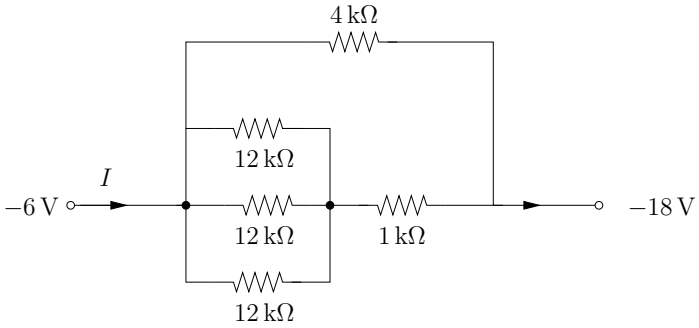
9. A fixed $1\,\mathrm{k\Omega}$ resistor is connected in series to a $4\,\mathrm{k\Omega}$ potentiometer (i.e., variable resistor). The series combination is connected to an ideal $5.0\,\mathrm{V}$ battery. Calculate the minimum and the maximum values of V_{AB} as the shaft of the potentiometer is rotated.



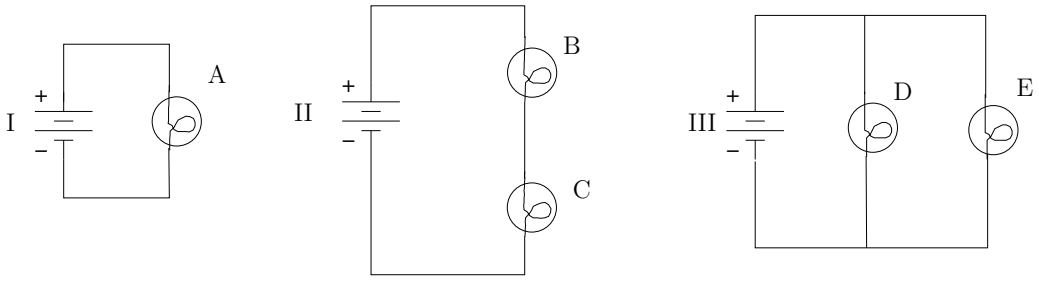
10. Calculate the voltage difference between points A and B. Which point is at a higher potential, A or B?



11. Calculate the current I in the illusrtated ciruit.



12. The illustrated circuits are built from a set of identical bulbs and identical (new) batteries. (Hint: Think of the bulbs as resistors.)



(a) Rank the five bulbs in order of brightness.

(b) Rank the batteries in order of how long they will last, from longest duration to shortest duration.

13. In the PHYS 212 DC Circuits lab you "played around" with batteries and light bulbs. One of the bulbs used in this lab was a CEC Industries Model 14 Miniature Incandescent Lamp; you can find a spec sheet for this lamp on the CEC web site: `http://ceclighting.com/`.

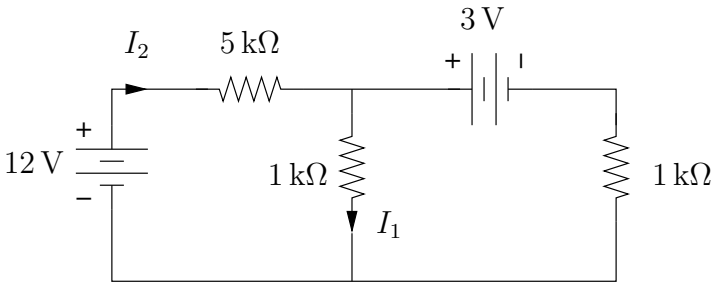
(a) Design a circuit with standard D cell batteries, resistors, and a Model 14 Lamp that will cause the lamp to be powered as it was designed to be used. How precise do your resistance values have to be?

(b) Approximately how long will the lamp stay lit if your circuit is left on continuously before the battery runs out? (You may have to look up some information.)

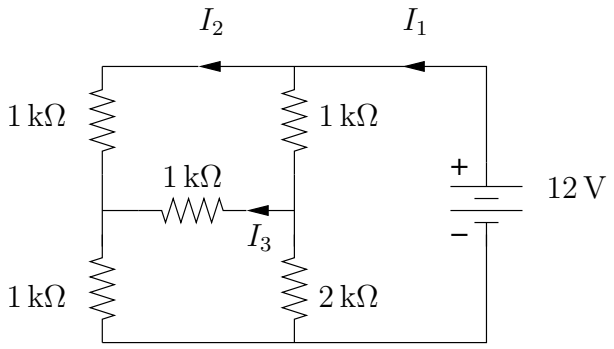
(c) Modify your circuit so that it powers two lamps. How long will the lamps stay lit in this circuit? (There is more than one way to do this.)

(d) What happens in your circuit if one of the bulbs burns out? Does the other stay lit? If not, modify your circuit so that the good bulb stays lit.

14. Calculate I_1 and I_2 in the illustrated circuit.



15. Calculate I_1, I_2, and I_3 in the illustrated circuit.

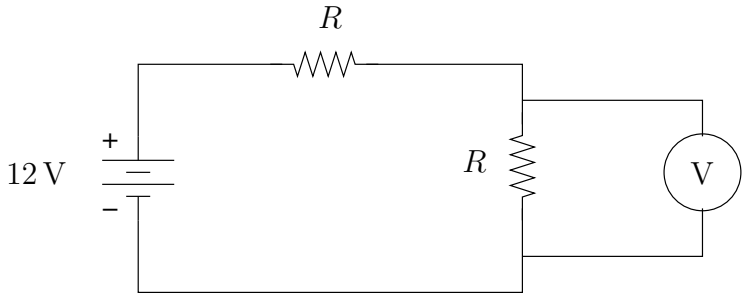


16. Describe an ideal voltage source and an ideal current source.

17. Assume that the voltmeter in the illustrated circuit is an oscilloscope with a 1 MΩ input impedance. (The input resistance of the scope is not shown in the figure.) Calculate the voltmeter reading for

    (a) $R = 1\,\text{k}\Omega$, and

    (b) $R = 1\,\text{M}\Omega$.



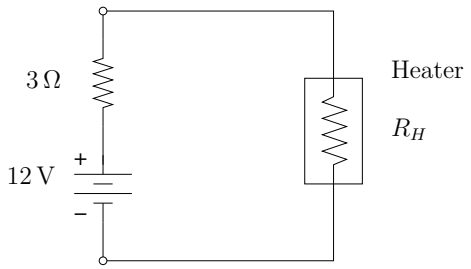
18. A 1 W, 1 kΩ carbon resistor carries a current of 30 mA. Calculate the power dissipated as heat in the resistor. Would this situation be desirable in a circuit?

19. An automobile battery has a terminal voltage of 12.8 V with no load. When the starter motor is being turned over it loads the battery, drawing 90 A of current, and the terminal voltage of the battery drops to 11 V. Calculate the internal resistance of the battery.

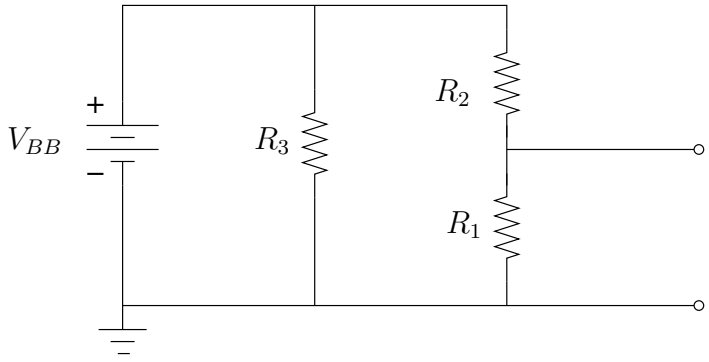
20. A 30 V DC power supply has an internal resistance of 2 Ω. Calculate the terminal voltage when the power supply is hooked up to a load resistor that draws a current of 500 mA from the supply.

21. Standard batteries are not ideal voltage sources; they can be modeled as an ideal voltage source V_S in series with an internal resistance R_{int}. When a battery goes bad, it's *not* because the value of V_S goes down, it's because R_{int} goes up. One consequence of this is that you can't use a standard voltmeter (like the ones you use in lab) to check if a battery is good. Explain why this is so, and describe qualitatively the characteristics of a meter that could check batteries.

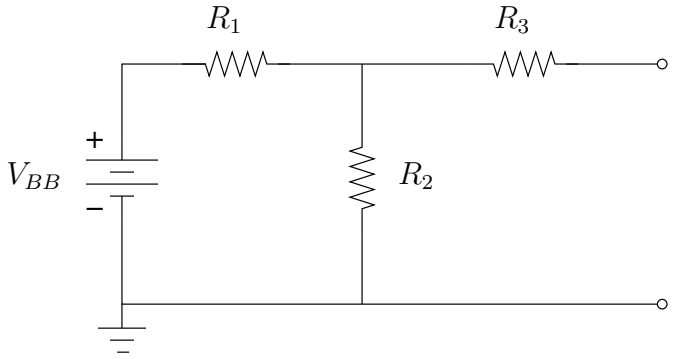
22. How large should the heater resistance R_H be to draw the most power from a 12 V battery with an internal resistance of 3 Ω? Calculate the power dissipated in the heater and in the battery under such conditions.



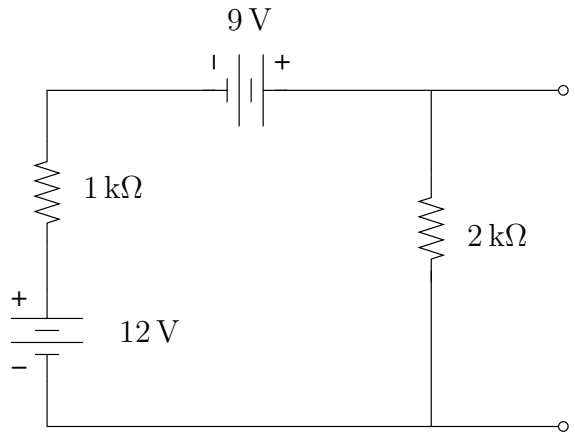
23. Determind the Thévenin equivalent for the illustrated circuit.



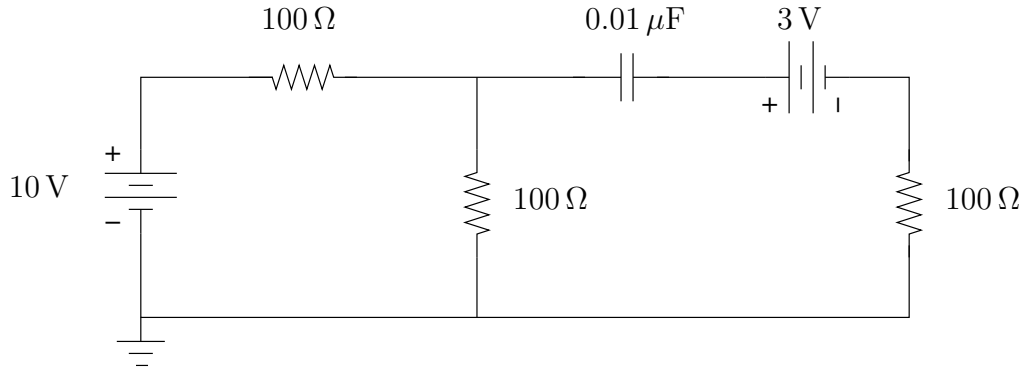
24. Determine the Thévenin equivalent of the illustrated circuit.



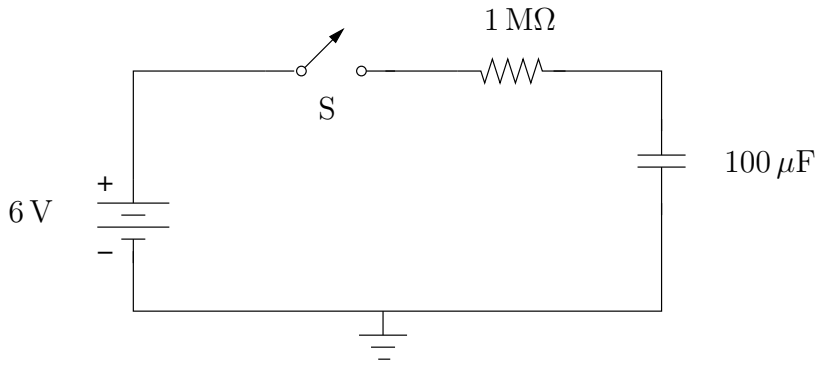
25. Calculate the Norton equivalent for the illustrated circuit at the indicated output terminals.



26. Consider the illustrated DC circuit. (All transients have died out, and the currents and charges have reached their equilibrium values.) Calculate the charge on the capacitor.

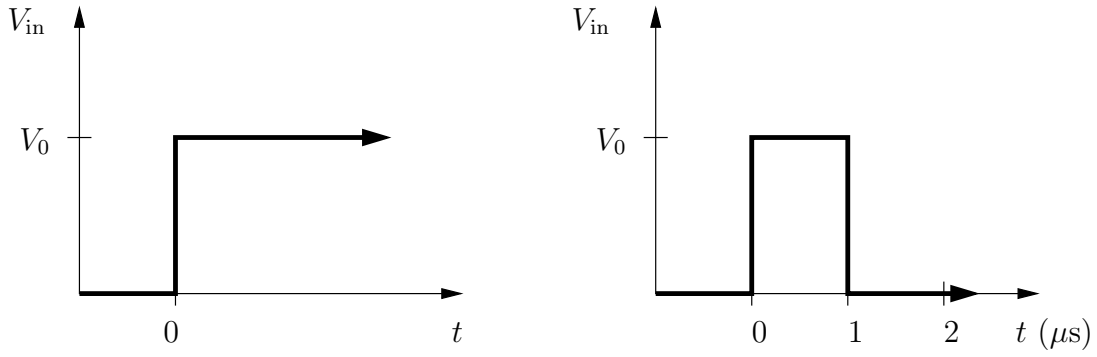


27. Consider the illustrated circuit that starts with the capacitor initially uncharged. The switch S is closed, and the capacitor begins to charge. What is the time interval between the time the capacitor is charged to 3 V and the time the capacitor is charged to 3.78 V?

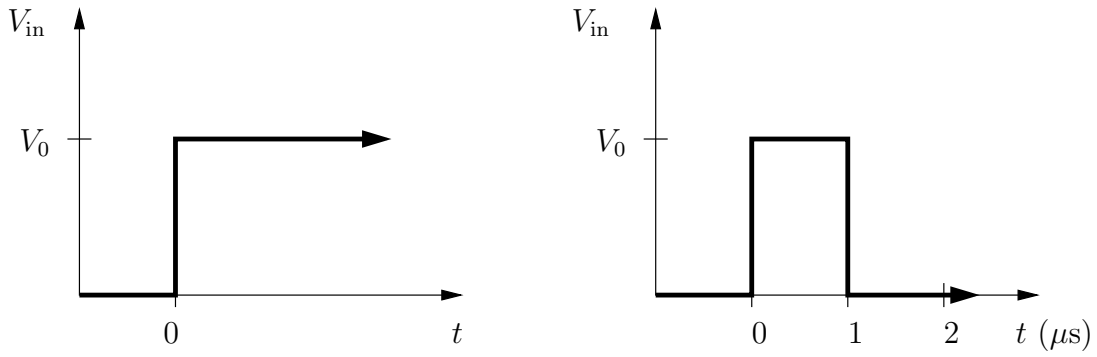


28. Prove that the 10% to 90% rise time for a RC low-pass filter is $2.2RC$ for a perfect step-function input.

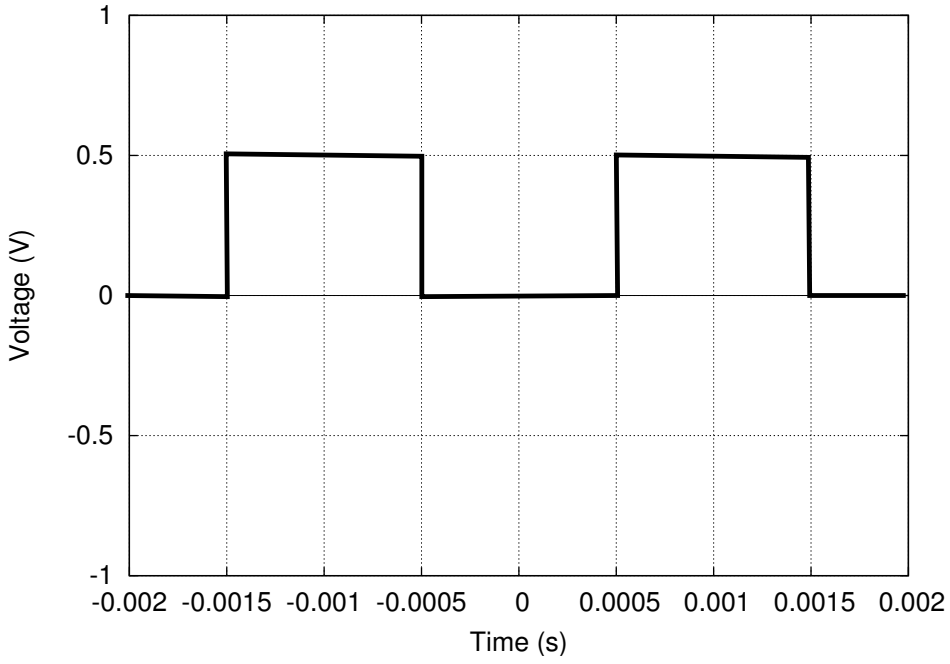
29. Sketch the approximate output from an RC integrating circuit (i.e., an RC low-pass filter) with $R = 10\,\text{k}\Omega$ and $C = 0.01\,\mu\text{F}$ for the illustrated inputs. For the input on the left, make sure that your sketch of the output has an appropriate time scale indicated on the axis.

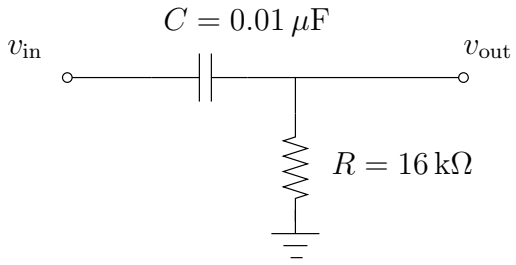


30. Sketch the approximate output from an RC differentiating circuit (i.e., an RC high-pass filter) with $R = 10\,\text{k}\Omega$ and $C = 0.4\,\text{nF}$ for the illustrated inputs. For the input on the left, make sure that your sketch of the output has an appropriate time scale indicated on the axis.



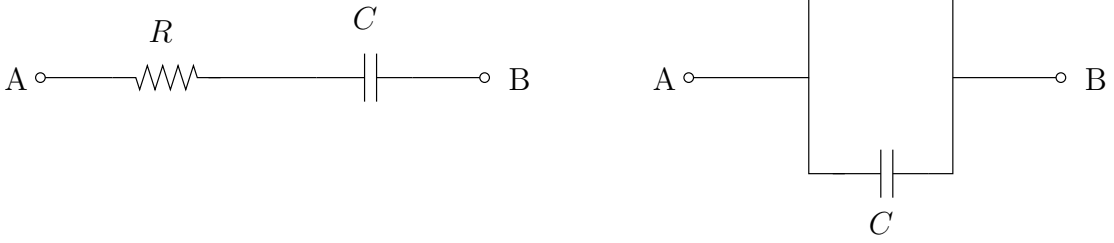
31. The graph below shows the input to the illustrated circuit. On the same graph sketch the output.





32. Calculate the capacitive reactance (i.e., magnitude of the impedance) in ohms of a $0.01\,\mu$F capacitor at (a) 100 Hz, (b) 1 kHz, (c) 100 kHz, (d) 1 MHz.

33. Calculate the impedance Z_{AB} in the forms $a + jb$ and $|d|e^{j\theta}$ for the two RC combinations illustrated, where a, b, and d represent real constants.



34. Design a high-pass filter with a breakpoint at 100 kHz.

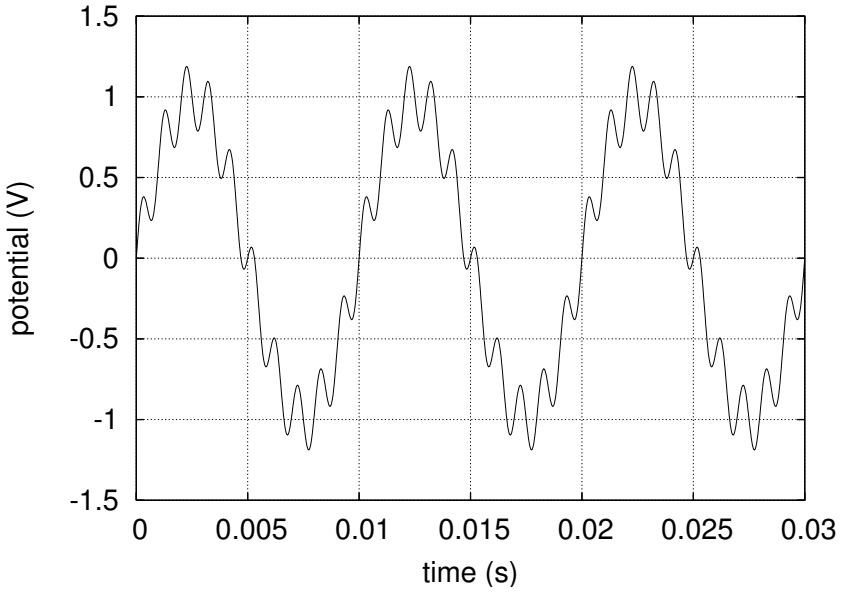
35. Design a low-pass RC filter that will attenuate a 60 Hz signal by 12 dB relative to the DC gain. Use a 100 Ω resistance.

36. For a low-pass RC filter prove that at the frequency $\omega = 2/RC$ the voltage gain equals $1/\sqrt{5} = 0.447$.

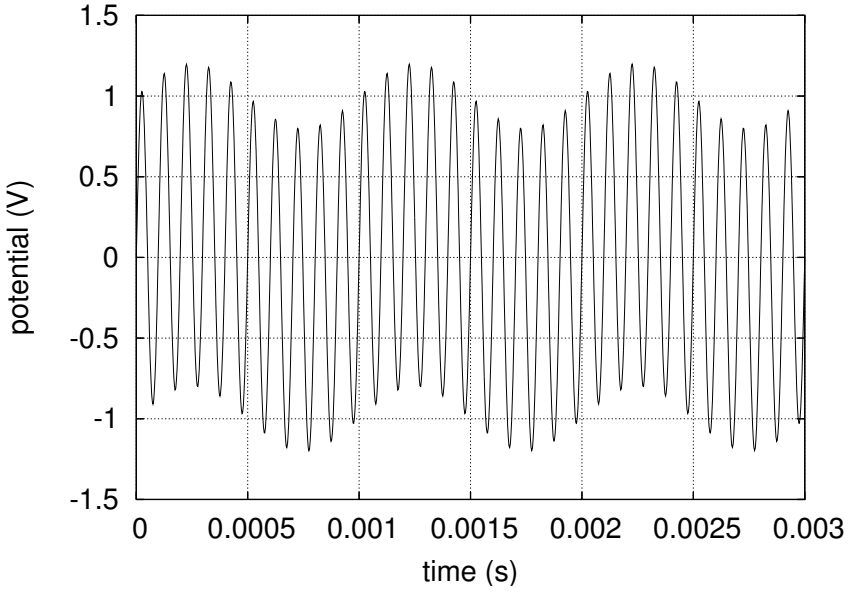
37. Draw the phasor voltage diagram for a high-pass filter for a frequency $\omega = 1/(RC)$. Your diagram should include phasors representing the input voltage $\tilde{v}_{\text{in}}$, the voltage across the resistor $\tilde{v}_R$, and the voltage across the capacitor $\tilde{v}_C$. Make sure all phasors have the correct relative lengths and correct angles with respect to each other. Use your diagram to calculate the phase shift of the output voltage relative to the input voltage.

38. Draw the phasor voltage diagram for a high-pass filter for a frequency $\omega = 1/(2RC)$. Your diagram should include phasors representing the input voltage $\tilde{v}_{\text{in}}$, the voltage across the resistor $\tilde{v}_R$, and the voltage across the capacitor $\tilde{v}_C$. Make sure all phasors have the correct relative lengths and correct relative angles. Use your diagram to calculate the phase shift of the output voltage relative to the input voltage.

39. The illustrated voltage vs. time graph is a combination of a signal and unwanted 1000 Hz noise. Design a filter that will significantly attenuate the 1000 Hz noise, but leave the signal unattenuated.

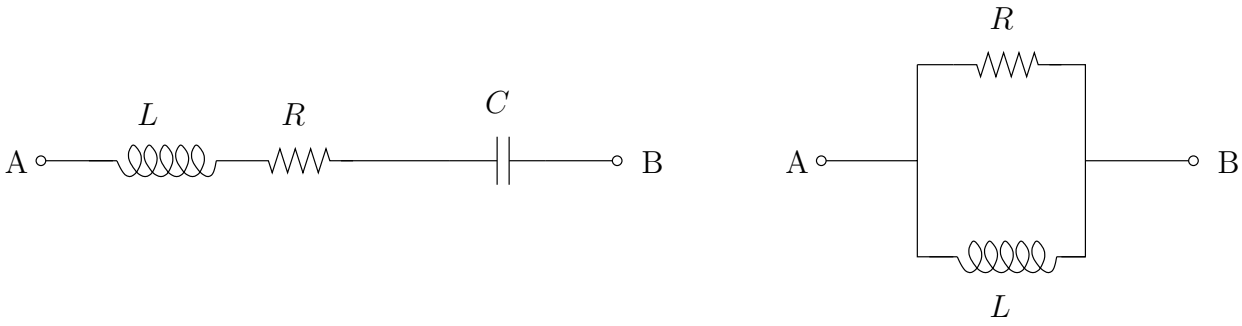


40. The illustrated voltage vs. time graph is a combination of a signal and unwanted 1000 Hz noise. Design a filter that will significantly attenuate the 1000 Hz noise, but leave the signal unattenuated.

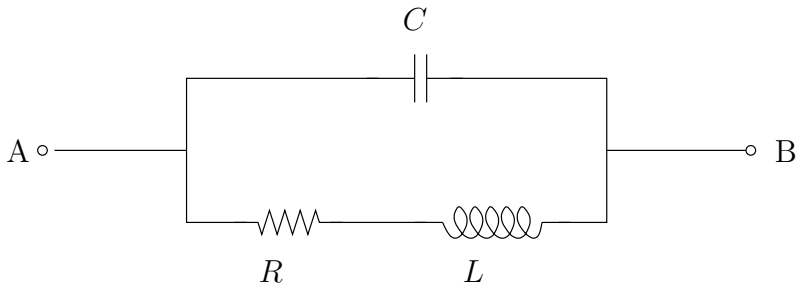


41. Calculate the inductive reactance (i.e., magnitude of the impedance) in ohms of a 2.5 mH coil at (a) 100 Hz, (b) 1 kHz, (c) 100 kHz, (d) 1 MHz.

42. Calculate the impedance Z_{AB} in the forms $a+jb$ and $|z|e^{j\theta}$ for the two RL combinations illustrated.

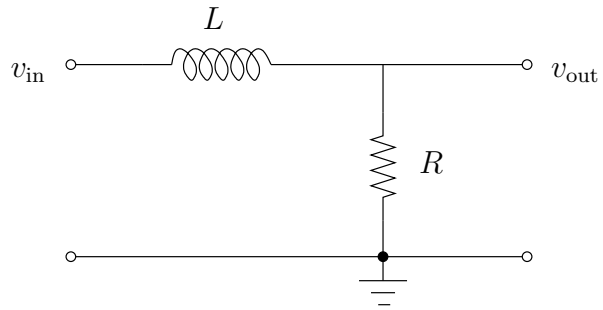


43. Calculate the impedance Z_{AB} in the form $a+jb$ for the illustrated RLC combination.

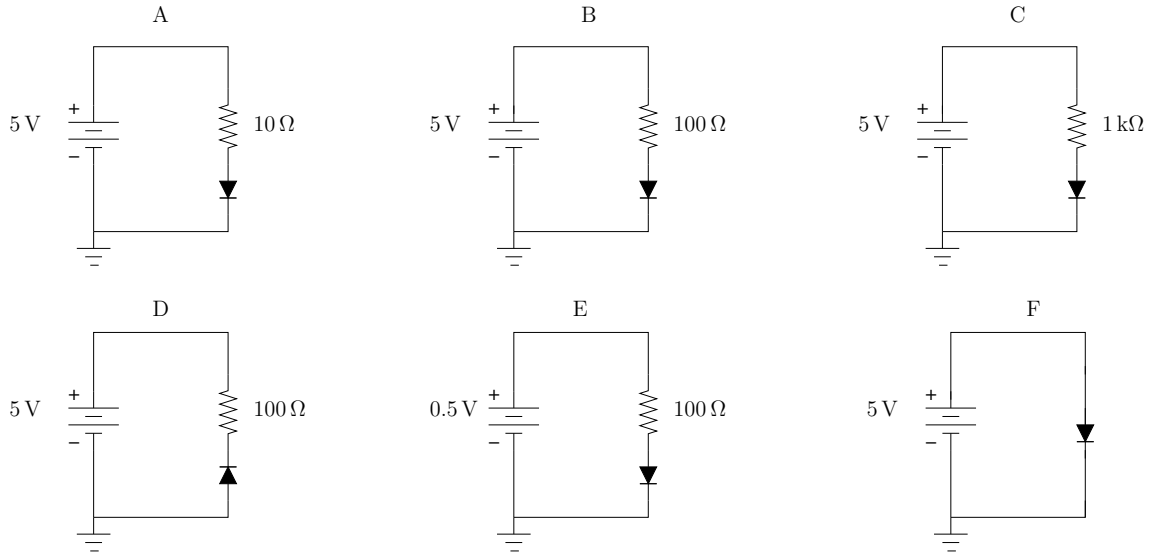


44. Sketch the phasor voltage diagram for a series RLC circuit at resonance.

45. Derive an expression for the voltage gain and the phase shift for the illustrated LR filter. Make a sketch of the gain vs. angular frequency.



46. Calculate the approximate current in the illustrated circuits containing a silicon diode.

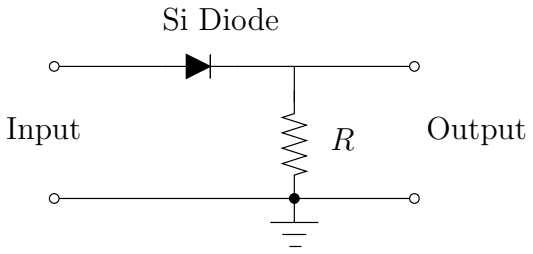


47. Repeat the previous problem for LEDs with a turn-on voltage of 2.5 V.

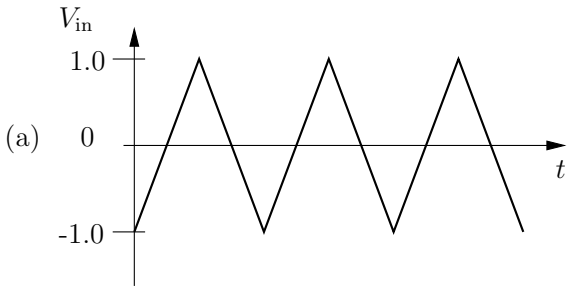
48. You want to design a circuit so that an LED with a turn-on voltage of 2.0 V and powered from a 5 V supply will run with a current of 15 mA. (The appropriate range of current for an LED is usually given in the specifications for a device when you buy it.) Choose an appropriate load-limiting resistor, and draw your circuit.

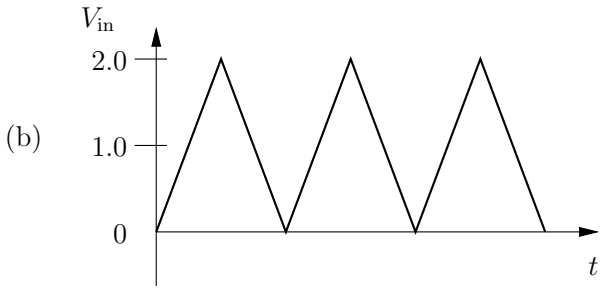
49. Design a diode clipping circuit to clip negative-going pulses so that the output is never more negative than −3 V.

50. Consider the illustrated circuit containing a silicon diode and a resistor.

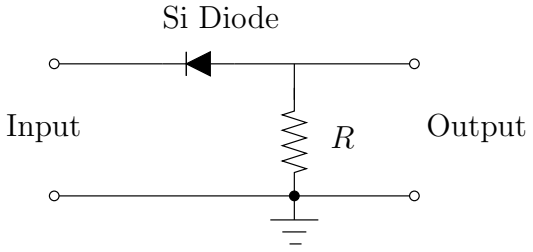


Sketch the voltage output waveform for each of the illustrated inputs.

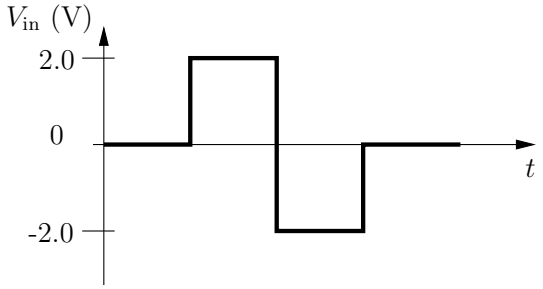




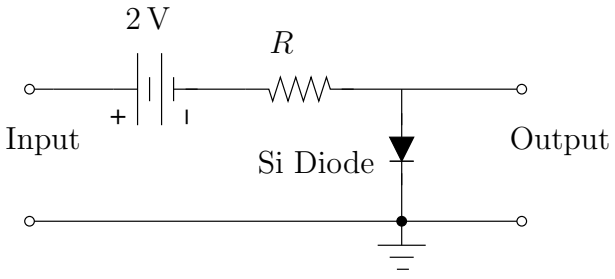
51. Consider the illustrated circuit containing a silicon diode and a resistor.



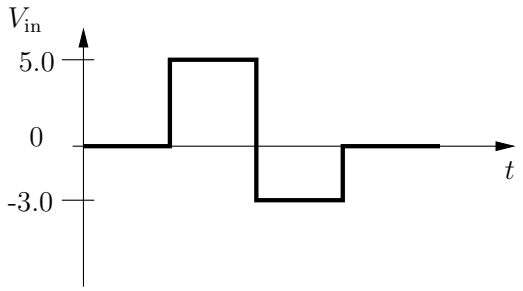
Sketch the voltage output waveform for the illustrated input.



52. Consider the illustrated circuit containing a battery, a silicon diode and a resistor.

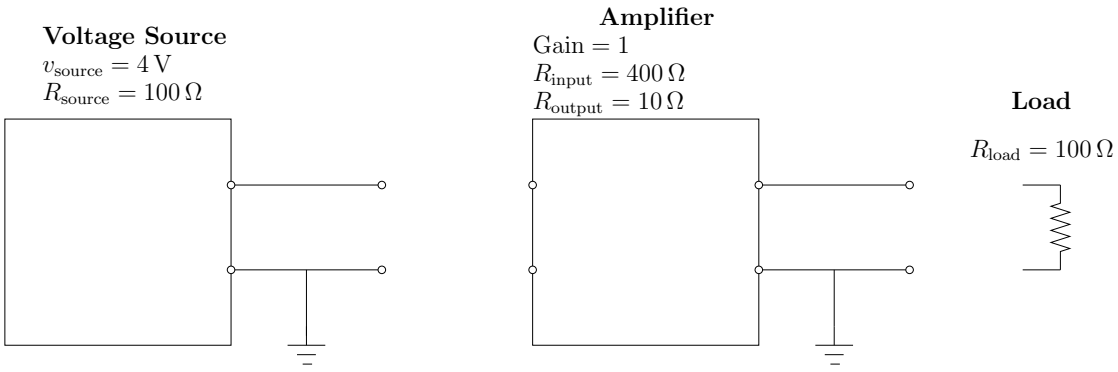


Sketch the voltage output waveform for the illustrated input.



53. Explain why the ripple amplitude in the output of an unregulated power supply increases as the load resistance is decreased.

54. Consider a voltage source with an open-circuit output of 4 V, and an output impedance of 100 Ω, an amplifier with a gain of 1, input impedance $R_{\text{input}} = 400\,\Omega$ and an output impedance $R_{\text{output}} = 10\,\Omega$, and a 100 Ω resistive load.

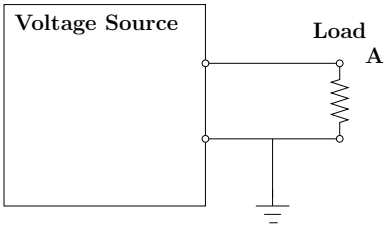


(a) When the load is connected directly to the source:

i. determine the voltage at point **A**,

ii. determine the current through the load, and

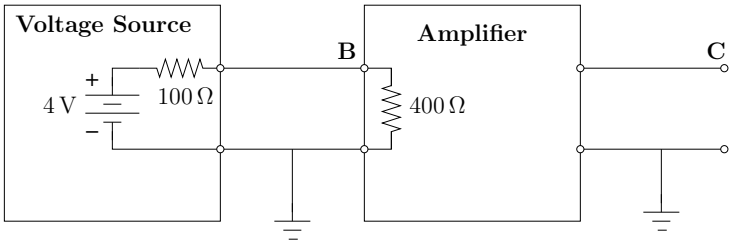
iii. determine the power dissipated in the load.



(b) When the amplifier is connected to the voltage source, but no load is attached:

i. determine the voltage at point **B** at the input to the amplifier, and

ii. determine the voltage at point **C** at the output of the amplifier.



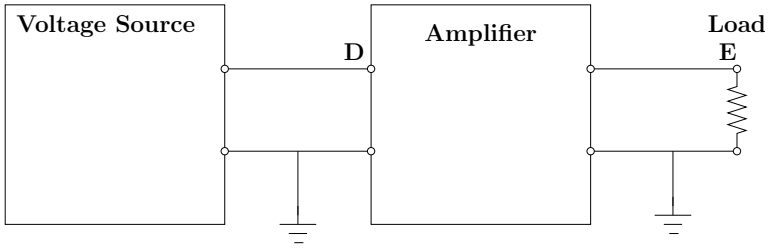
(c) When the amplifier is connected to the voltage source, and the load is connected across the output of the amplifier:

i. determine the voltage at point **D** at the input of the amplifier,

ii. determine the voltage at point **E**,

iii. determine the current through the load, and

iv. determine the power dissipated in the resistor.



(d) Repeat the previous calculations for the loaded amplifier, except this time assume the the amplifier has an input impedance $R_{\text{input}} = 10\,\text{k}\Omega$ and an output impedance $R_{\text{output}} = 1\,\Omega$.

55. A "black box" with three terminals labeled E, B, and C is connected in the following illustrated circuit.

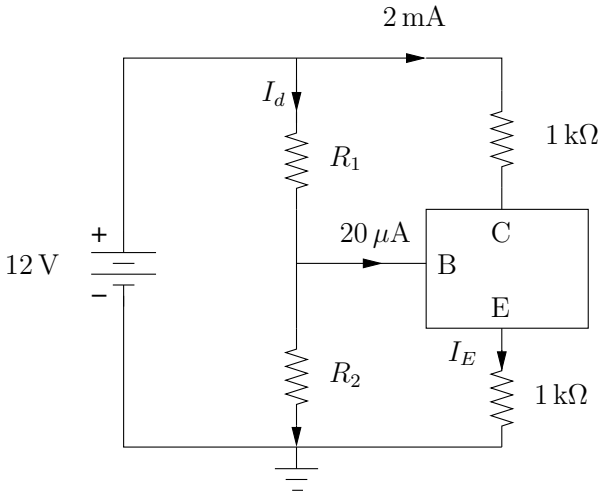
    (a) Calculate I_E.

    (b) Calculate V_C and V_E.

    (c) If terminal B is 0.6 V more positive than terminal E, calculate the approximate ratio of R_1 and R_2, assuming that I_d is very large compared to the 20 μA flowing in the B lead.

    (d) Calculate the approximate power dissapated in the "black box."

    (The "black box" is a silicon NPN transistor.)



56. (a) Write a simple formula that expresses the relationship between I_C, I_B, and I_C in a bipolar transistor.

    (b) Write an expression for I_C as a function of I_B and α.

    (c) Write an expression for I_C as a function of I_B and β.

    (d) Write an expression for I_C as a function of I_E and α.

    (e) Write an expression for I_C as a function of I_E and β.

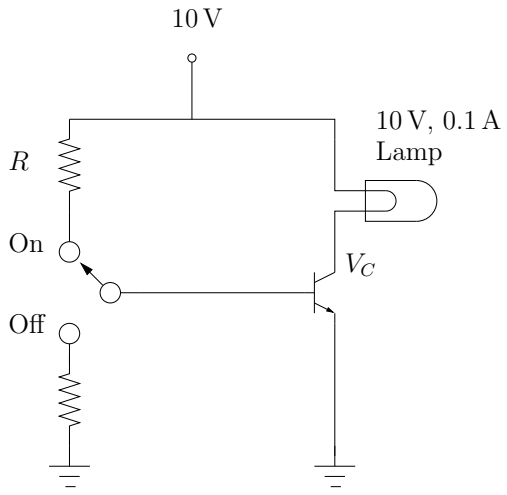
    (f) Write an expression for I_B as a function of I_E and α.

    (g) Write an expression for I_B as a function of I_E and β.

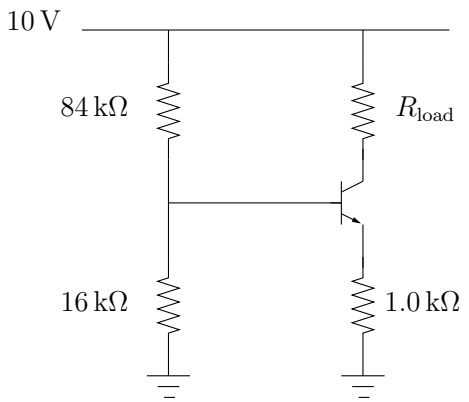
57. Fill in the blanks: The base voltage of an "on" silicon NPN transistor is always approximately _____ more _____ than the emitter.

58. Consider the illustrated circuit in which a mechanical switch is used to turn on a small control current that activates the transistor "switch" that enables a much larger current through the lamp. The manufacturer says that the lamp was desigend for 1 V, 0.1 A operation; for the purposes of this exercise consider the lamp as a simple resistor of with $R_{\text{lamp}} = 100\,\Omega$, and assume that $\beta = 100$ for this transistor. Fill in the following table giving the the base current I_B, the collector current I_C and the voltage at the collector V_C for the indicated values of R. For which resistor(s) will the lamp light be powered as it was designed to be?

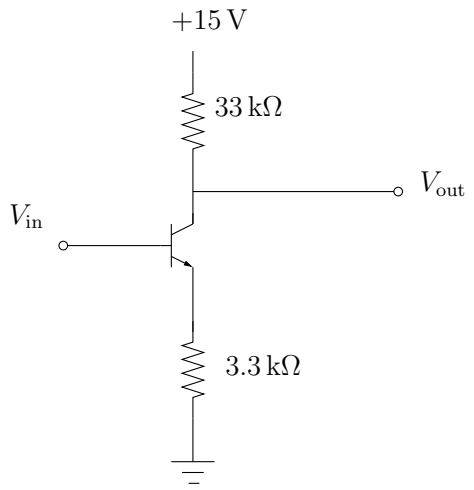
R	I_B	I_C	V_C
100 kΩ			
10 kΩ			
1 kΩ			



59. Calculate the current through the load resistor R_{load} in the illustrated circuit. (Use the "simplest" model of the transistor.) Does your result depend on the value of R_{load}?



60. Consider the simple common-emitter amplifier discussed in class. (This is also part of the amplifier that some of you built in the optional part of the Introduction to Transistors Lab.) Consider as the input the voltage $V_{\text{in}} = 1.59 + 0.33\cos(\omega t)$, i.e., a signal that oscillates between $1.59 - 0.33 = 1.26\,\text{V}$ and $1.59 + 0.33 = 1.92\,\text{V}$.

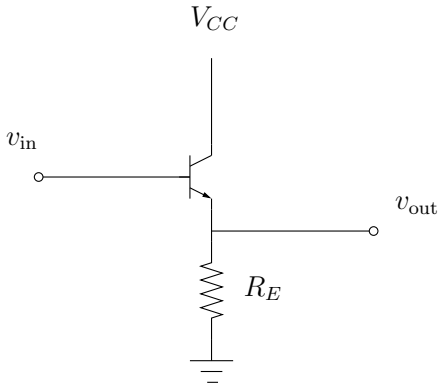


(a) Use the "simplest model" of transistors to calculate V_{out} when $V_{\text{in}} = 1.26\,\text{V}$.

(b) Use the "simplest model" of transistors to calculate V_{out} when $V_{\text{in}} = 1.92\,\text{V}$.

(c) Using the results you obtained in the previous parts of this problem determine the voltage gain for AC signals ($\Delta V_{\text{out}}/\Delta V_{\text{in}}$).

61. In class we showed that the input impedance of the simple voltage follower shown below is $(\beta + 1)R_E$. Show that the output impedance is given by $R_{\text{source}}/(\beta + 1)$, where R_{source} is the output impedance of the source that is providing v_{in}. Remember that the output impedance is $\Delta v_{\text{out}}/\Delta i_{\text{out}}$.



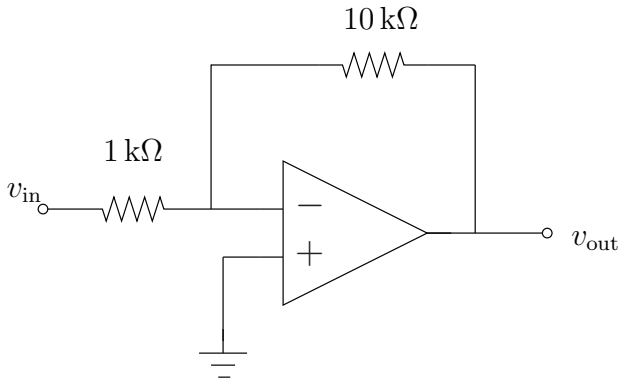
62. State the two rules for ideal op-amp behavior when the op-amp is hooked up with negative feedback.

63. For the illustrated amplifier, determine

    (a) the voltage gain A_v,

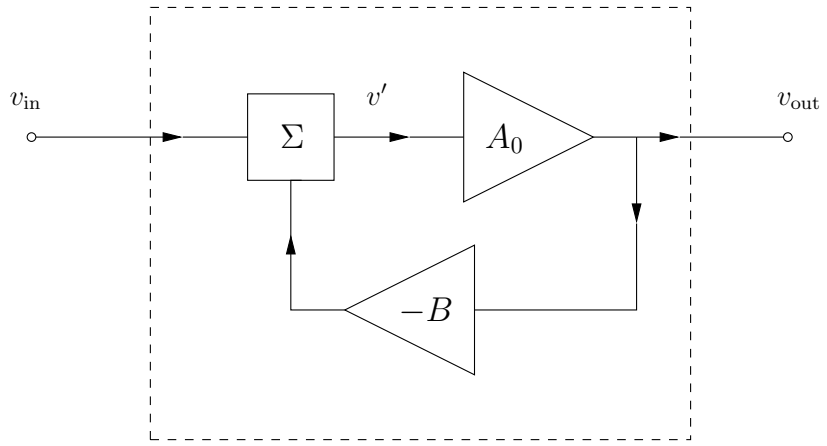
    (b) the input impedance, and

    (c) the qualitative effect on sinusoidal signals of adding a 1600 pF capacitor in parallel with the 10 kΩ resistor.



64. Why is an amplifier with a voltage gain of 1 (i.e., with $v_{\text{out}} = v_{\text{in}}$) of any use to anyone?

65. Consider the simple generalized negative feedback amplifier discussed in class.



(a) Derive the expression that gives the closed-loop gain A_v in terms of the open-loop gain A_0 and the percentage of the output B fed back into the summming amplifier.

(b) Show using specific numerical values in your formula that if $A_0 = 10^6$ and $B = 0.01$, then a 20% change in A_0 results in a 0.002% change in A_v.

(c) Prove that a fractional change in the open-loop gain $\Delta A_0/A_0$ results in an approximate fractional change in the closed-loop gain given by

$$\frac{\Delta A_v}{A_v} \simeq \frac{1}{(1 + A_0 B)} \frac{\Delta A_0}{A_0} \simeq \frac{1}{A_0 B} \frac{\Delta A_0}{A_0}.$$

66. (a) Explain why negative feedback will increase rather than decrease the input impedance of an amplifier.

(b) Explain why a large input impedance is usually desirable.

67. Design an amplifier with op-amps that takes four inputs v_A, v_B, v_C, and v_D, and produces an output $v_{\text{out}} = v_A + 2v_B + 4v_C + 8v_D$.

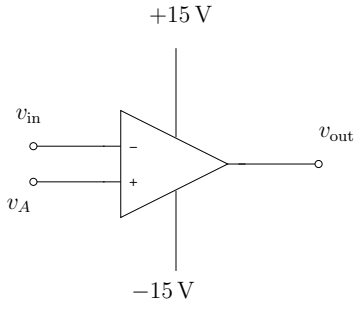
68. Design an op-amp amplifier that will give a constant current I_L through a load resistance, independent of the value R_L of the load resistance; the output current should be proportional to the input voltage. Choose component values that will give a current I_L of 1 mA for a 10 mV input. Explain why your circuit works. (Look back at the transistor current source for ideas.)

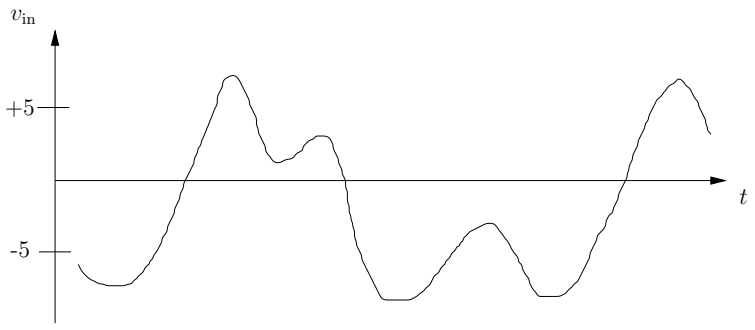
69. (a) Design a current-to-voltage converter to convert a $1\,\mu$A DC input current from a constant current source into a $2\,$V signal.

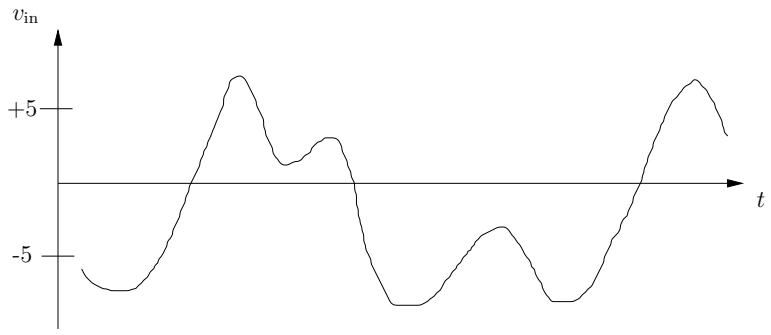
(b) Now consider an AC input current with an amplitude of $1\,\mu$A and a frequency of $100\,$HZ. There is also AC noise present at $10,000\,$Hz. Redesign your current-to-voltage converter so that your output voltage has an amplitude of $2\,$V, and the noise is significantly attenuated.

70. (a) Sketch the output v_{out} of the illustrated op-amp when $V_A = +5\,$V.

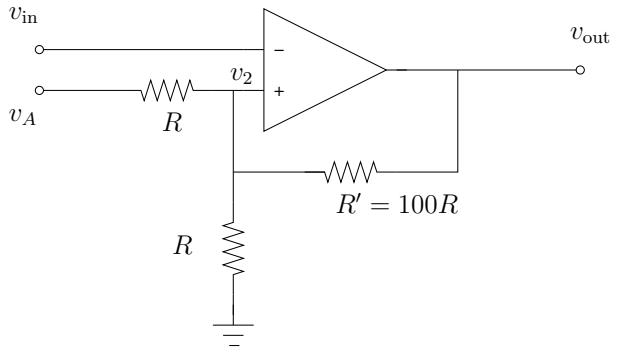
(b) Sketch the output v_{out} of the illustrated op-amp when $V_A = -5\,$V.







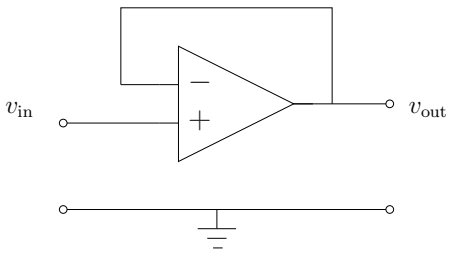
71. In lab you investigated the operation of a Schmitt trigger. Your trigger made transitions at reference voltages that were near 0 V. In the illustrated circuit the transitions have been shifted away from zero because of the voltage v_A. Determine the transition voltages for this more general Schmitt trigger. Express your answer in terms of v_A, R, and the saturation voltage of the op-amp V_{CC}. (You may assume that the negative saturation voltage is $V_{EE} = -V_{CC}$).



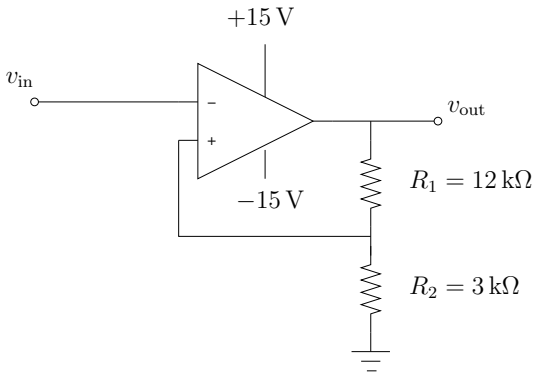
72. Ideal op-amps are assumed to have open-loop gains A_0 that are infinite, and this infinite open-loop gain leads to equal voltages at the inverting and non-inverting inputs (when the op-amp is placed in a circuit with negative feedback). The following circuit is a voltage follower, and for an ideal op-amp $v_{\text{out}} = v_{\text{in}}$. For this problem assume that the op-amp is **not** ideal, and A_0 is finite. (All other properties of the op-amp may be assumed to be ideal; for example, you may still assume that the inputs draw no current.)

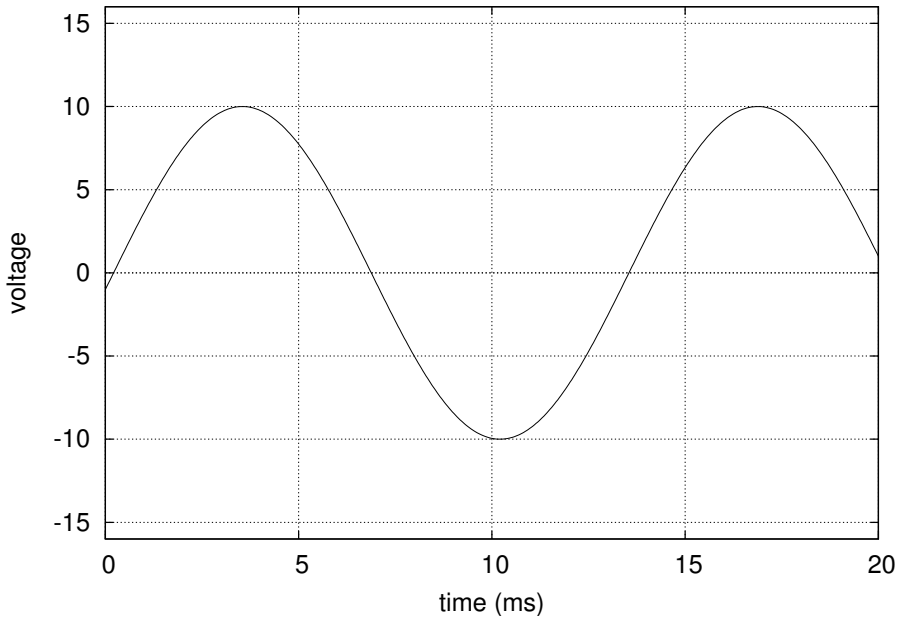
    (a) Determine v_{out} in terms of v_{in} and A_0. Show that you recover the ideal op-amp result in the limit $A_0 \to \infty$.

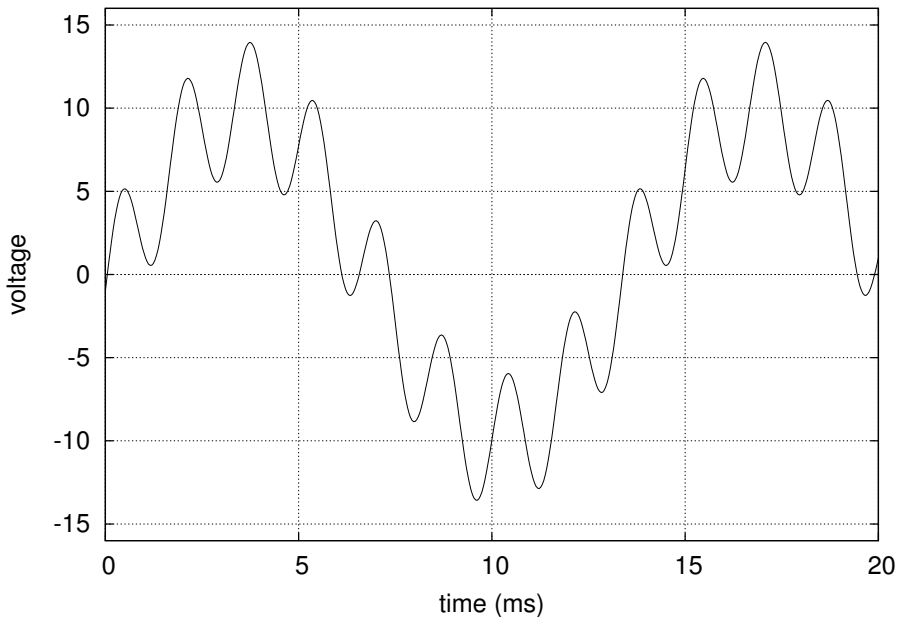
    (b) Determine the potential difference at the inputs, $v_2 - v_1$. Show that you recover the ideal op-amp result in the limit $A_0 \to \infty$.



73. Sketch the output v_{out} of the illustrated op-amp for the two illustrated inputs.

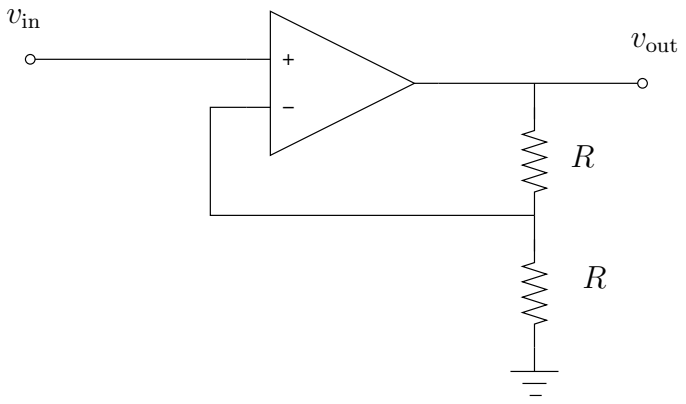




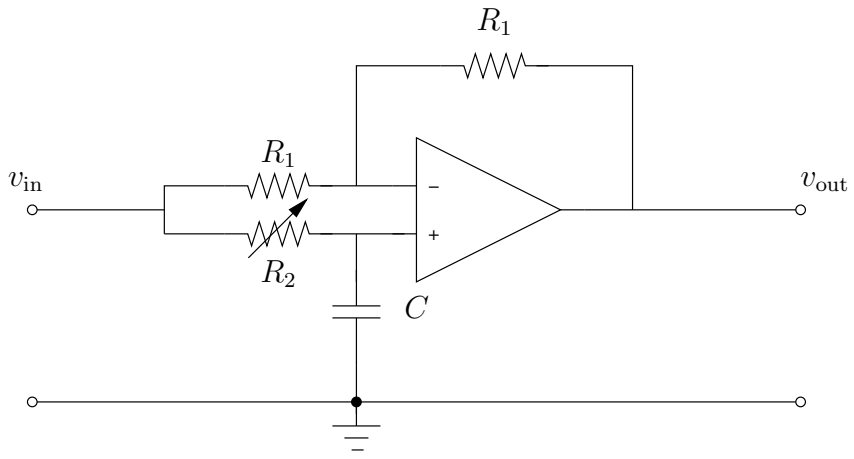


74. (a) Assume that the op-amp in the illustrated circuite is ideal and determine an expression for the gain of the illustrated circuit.

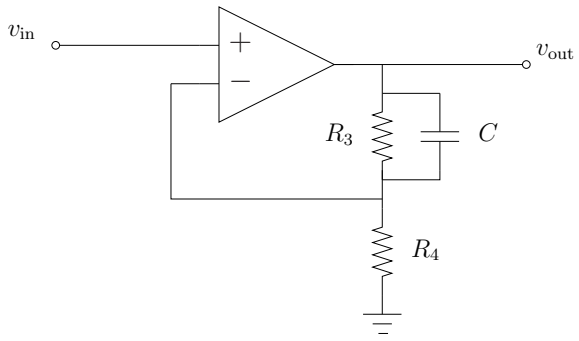
(b) Assume the that illustrated op-amp is **not** ideal in one respect: the open-loop gain A_0 is **not** infinite. Determine an expression for the gain of the circuit. (This result should reduce to your previous result in the limit $A_0 \to \infty$.)



75. What does the illustrated circuit do? (Consider a sinusoidal input v_{in}, and determine v_{out}.) There is a nice formula that gives the output as a general function of input frequency ω, R_2, and C, but it might be easier to start by calculating the output for the specific values $\omega = 2\pi \times 10^3\,\text{s}^{-1}$, $C = 10\,\text{nF}$, and $R_2 = 15.915\,\text{k}\Omega$.



76. The illustrated amplifier is a slight modification of a circuit that should be familiar to you.

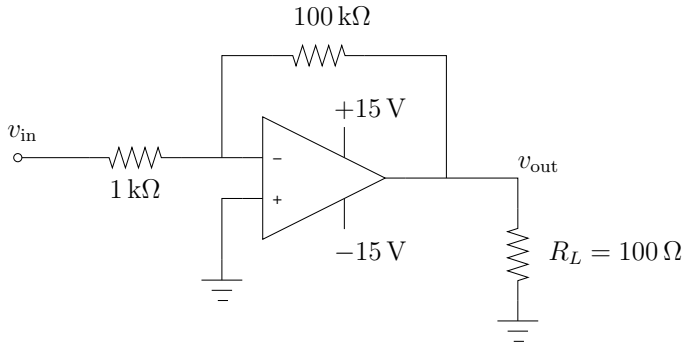


(a) What is the gain of the amplifier A_v for DC signals, i.e., when $\omega = 0$? (You should be able determine this from applications of derivations done previously in class and lab.)

(b) What is the gain of the amplifier A_v for sinusoidal AC signals when $\omega \to \infty$? (You should be able determine this from applications of derivations done previously in class and lab.)

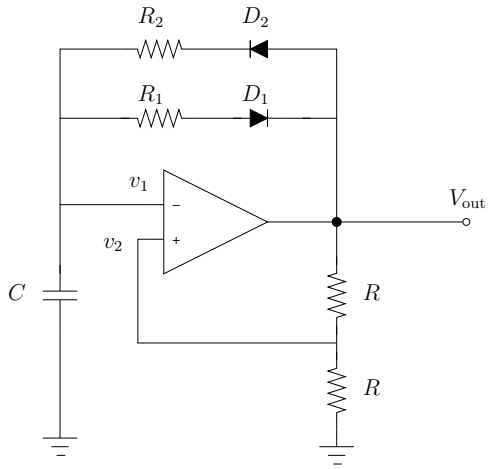
(c) What is the gain of the amplifier A_v when $\omega = 1/(R_3C)$?

77. The output impedance of most op-amps is *extremely* low when negative feedback is used. When you tried to determine the output impedance in lab by decreasing the value of the load resistance R_L (the way you did with voltage dividers) you probably saw something go "wrong" with the sinusoidal signal output voltage v_{out} before the amplitude dropped to half of its open-circuit value. Typical inexpensive op-amp chips can supply a maximum current of approximately 25 mA, and if they are used in a way that calls for more current, the output wave is distorted. (One manifestation in lab was a flat-topped sine wave that looked like clipping.) Calculate the maximum amplitude sinusoidal input that will produce a non-distorted output across a load resistor $R_L = 100\,\Omega$ in the illustrated circuit. Repeat your calculation for $R_L = 1\,\text{k}\Omega$.



78. Make a qualitative sketch of v_1, v_2, and v_{out} vs. time for the illustrated circuit for the following two cases:

- $R_2 = 2R_1$, and
- $R_2 = R_1/2$.



79. Convert the following binary number to decimal:

$$(10110)_2 = (\_\_\_\_\_)_{10}$$

80. Convert the following decimal number to binary:

$$(49)_{10} = (\_\_\_\_\_)_2$$

81. Convert the following decimal number to hexadecimal:

$$(49)_{10} = (\_\_\_\_\_)_{16}$$

82. Convert the following hexadecimal number (base 16) to decimal:

$$(3F2)_{16} = (\_\_\_\_\_)_{10}$$

83. Convert the following decimal number to binary coded decimal (BCD):

$$(63)_{10} = (\_\_\_\_\_)_{\text{BCD}}$$

84. Convert the following binary coded decimal (BCD) number to decimal:

$$(1001\,0111)_{\text{BCD}} = (\_\_\_\_\_)_{10}$$

85. Write the truth tables for the following functions of two binary variables, and sketch the standard gate symbol. (You should be able to do this without looking them up.)

    (a) AND

    (b) NAND

    (c) OR

    (d) NOR

    (e) XOR

    (f) XNOR

86. Draw a schematic diagram showing how you would implement the following functions using only NAND gates.

(a) $F = \overline{A}$

(b) $F = A + B$

(c) $F = A \cdot B$

(d) $F = A \cdot \overline{B} + \overline{A} \cdot B$

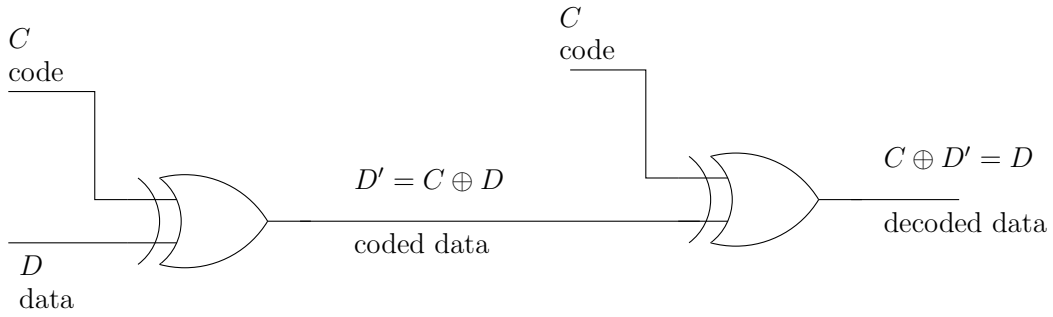
87. An XOR gate can be used to encode and decode data. Let's work through a simple example.

(a) The ASCII code (American Standard Code for Information Interchange) is a common case-sensitive *alphanumeric* code that represents letters as numbers. Find an ASCII table and translate the the word "Hi" into a decimal number and a binary number:

$$\text{Hi} \longrightarrow (\_\_\_\_\_)_{10} = (\_\_\_\_\_)_2$$

(b) Imagine that the binary ASCII code for "Hi" is translated into a string of pulses that are fed to the data input in the circuit below. At the same time a string of coding pulses are fed to the C input. Determine the binary number that represents the coded data D' if the code is 01110100110111.

(c) Verify that the second XOR gate returns the original message.



88. Design a flip-flop (latch) using cross-coupled NOR gates instead of the cross-coupled NAND gates you used in lab. (You should be able to do this without using any "external" resources, but if you get stuck you can look this up in your text or on-line.) Give the truth table for your flip-flop. Should your inputs be labeled (S, R), or ($\overline{S}$, $\overline{R}$)?

89. (a) Show that the operation of an XOR gate ($A \oplus B$) can be written as

$$A \oplus B = A \cdot \overline{B} + \overline{A} \cdot B.$$

(b) Based on this identity, draw a circuit diagram showing how to realize an XOR gate using only NAND gates.

90. (a) Show that the operation of an XOR gate ($A \oplus B$) can be written as

$$A \oplus B = (A + B) \cdot (\overline{A \cdot B})$$

(b) Based on this identity, draw a circuit diagram showing how to realize an XOR gate using only NAND gates. (This should be a different circuit than the one drawn for the previous problem).

91. Table 8.3 on p. 209 of Eggleston, (or Table 12.8 on p. 540 of Simpson, or ...) gives several Properties of Boolean Operations. By examining the truth tables for the AND and the OR gates you should be able to convince yourself that *all* of these relationships are true. Specifically, give arguments that demonstrate that

(a) $A + \overline{A} = 1$, and

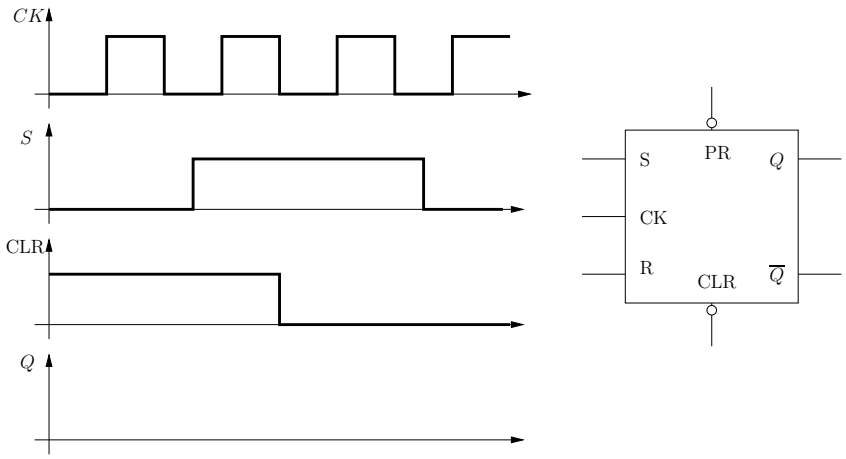
(b) $A \cdot A = A$.

92. There are many commutative, distributive, and associative rules for Boolean operations. **NOTE:** In Boolean expressions there are often some suppressed parentheses and implied order of operations, just like there are for normal addition and multiplication. For example $A + \overline{A} \cdot B$ means $A + (\overline{A} \cdot B)$, and *not* $(A + \overline{A}) \cdot B$. Write out truth tables that demonstrate that

(a) $A \cdot (\overline{A} + B) = A \cdot B$, and

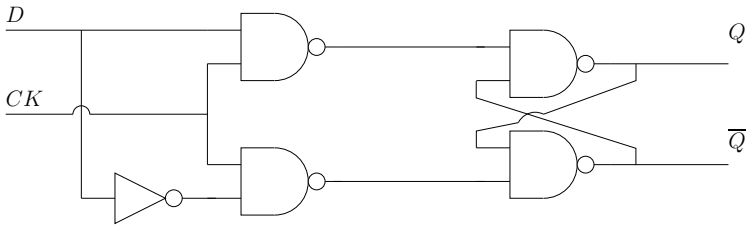
(b) $A + A \cdot B = A$

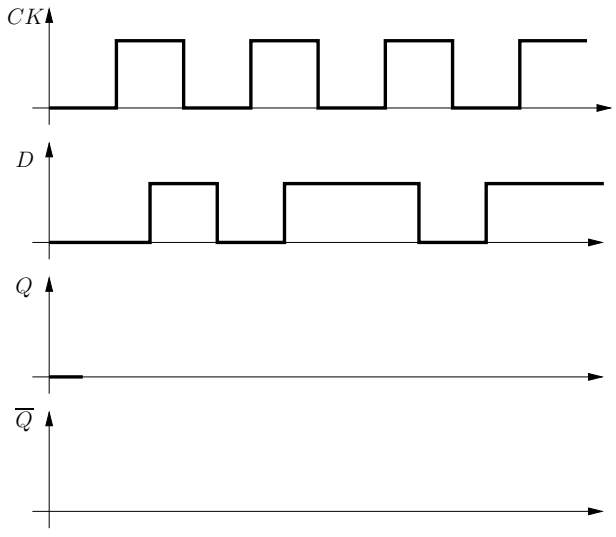
93. Sketch Q for the illustrated clocked RS flip-flop. The flip-flop PRESET and CLEAR are asynchronous. This means that they act like a SET and RESET that override the clock. Note that PRESET and CLEAR inputs are active-low.



94. (a) Write the truth table for the illustrated circuit.

    (b) Complete the timing diagram.

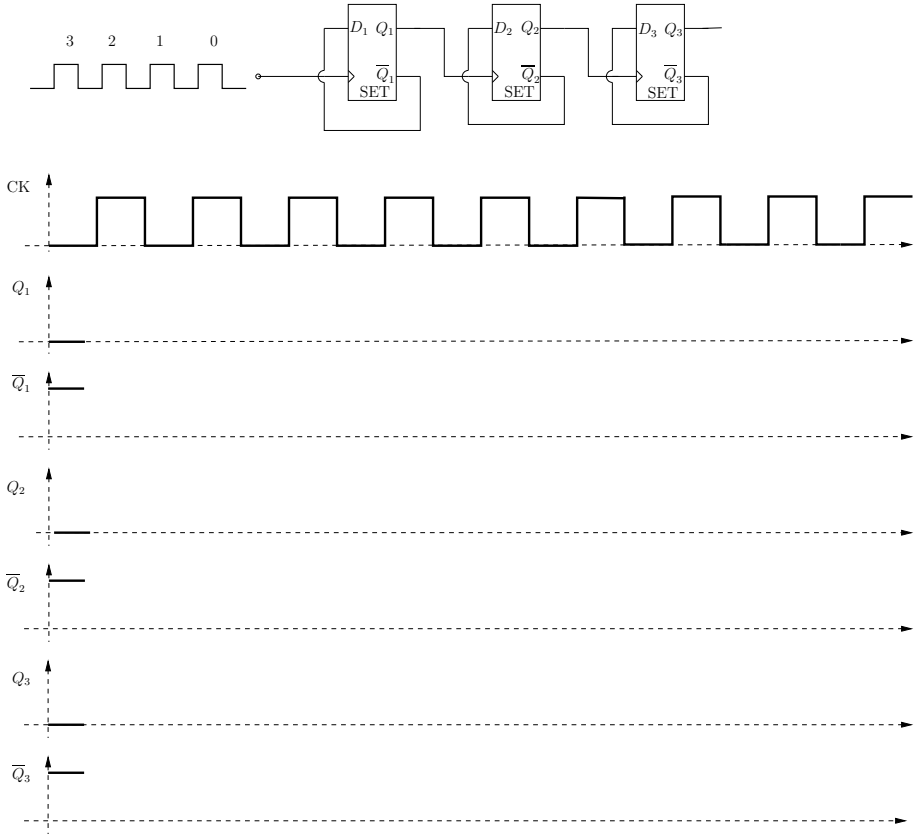




95. The illustrated circuit is made of positive edge-triggered type D flip-flops.

(a) Complete the timing diagram for the circuit.

(b) If you consider $\overline{Q}_3\overline{Q}_2\overline{Q}_1$ as a binary number, what is the counting sequence for the circuit.

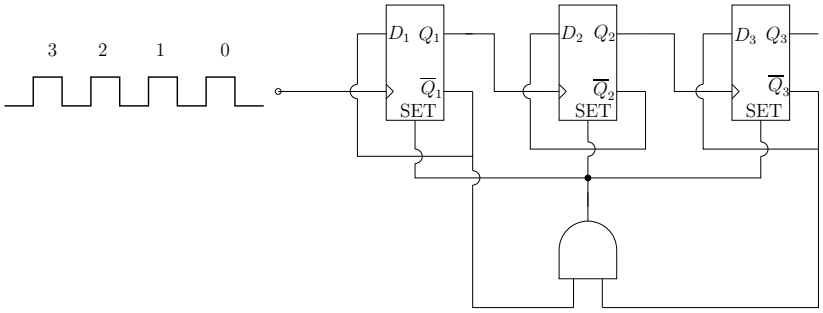


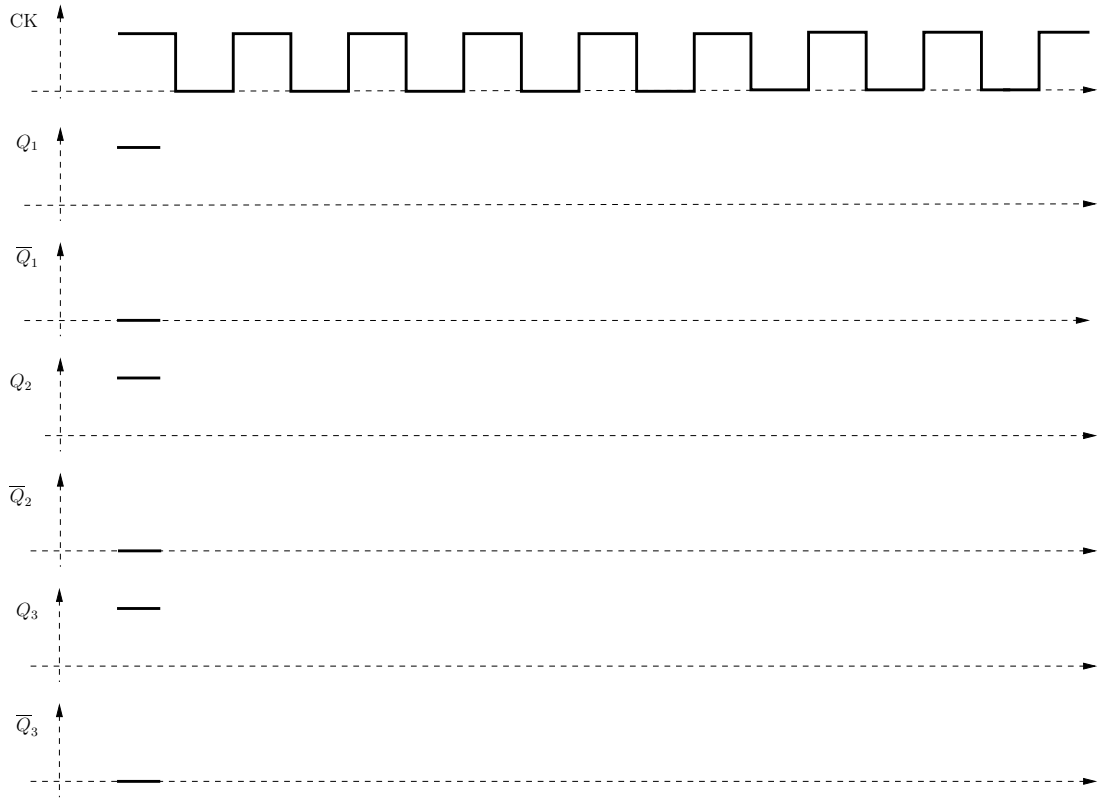
96. In lab you built a one-shot from a 555 timer chip: you connected a resistor R between 5 V and pins 6 & 7, and you connected a capacitor C between pins 6 & 7 and ground. Show that the duration of the pulse from this one-shot is $1.1RC$.

97. The illustrated circuit is made of positive edge-triggered type D flip-flops and an AND gate.

(a) Complete the timing diagram for the circuit. (You may need to consult the *CMOS Cookbook*).

(b) If you consider $\overline{Q}_3\overline{Q}_2\overline{Q}_1$ as a binary number, what is the counting sequence for the circuits.

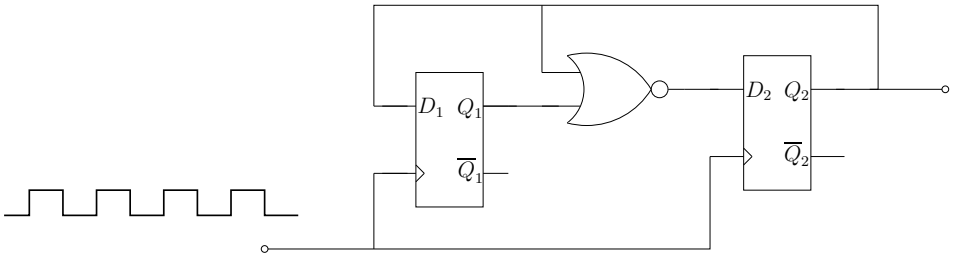


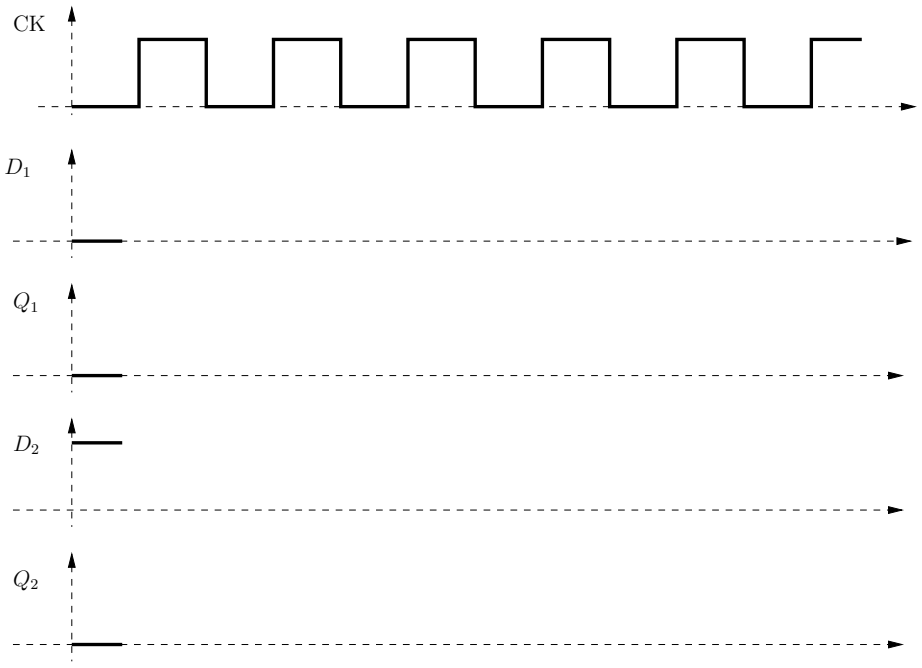


98. The illustrated circuit is made of 2 positive edge-triggered type D flip-flops and a NOR gate. Notice that the clock is applied simultaneously to both flip-flops, which makes this is an example of a *synchronous* counter in which all outputs change simultaneously. (In lab you built a *ripple*, or *asynchronous* counter, in which the output of one flip-flop serves as the clock for the next flip-flop.)

(a) Complete the timing diagram for this counter.

(b) In lab you built what are known as divide-by-2 counter and a divide-by-4 counters. What's a good name for the counter of this problem?





99. Consider an eight-bit single-slope A/D converter with $V_{\text{ref}} = 5\,\text{V}$ and $T_{\text{clock}} = 1\,\mu\text{s}$. Imagine that the converter is used to digitize an input signal of $v_{\text{in}} = 5\,\text{V}$.

    (a) If $R_{\text{integrator}} = 10\,\text{k}\Omega$, and $C_{\text{integrator}} = 0.01\,\mu\text{F}$, what is the digital output?

    (b) If $R_{\text{integrator}} = 100\,\text{k}\Omega$, and $C_{\text{integrator}} = 0.01\,\mu\text{F}$, what is the digital output?

100. Consider an eight-bit version of the dual-slope A/D converter you built in lab with $V_{\text{ref}} = 5\,\text{V}$, $T_{\text{clock}} = 1\,\mu\text{s}$, $R_{\text{integrator}} = 10\,\text{k}\Omega$, and $C_{\text{integrator}} = 0.01\,\mu\text{F}$. Imagine that the converter is used to digitize an input signal of $v_{\text{in}} = 1.25\,\text{V}$. What is the digital output?

101. If the most significant bit (MSB) of an eight-bit A/D converter corresponds to an input voltage of 5 V,

    (a) What range of analog input voltage will produce an output of 10100101?

    (b) What will the digital output be for an analog input of 8.75 V?

102. If the most significant bit (MSB) of an eight-bit D/A converter corresponds to an output voltage of 5 V,

    (a) What is the analog output for a digital input of 01100101?

    (b) What is analog output for a digital input of 10010000?

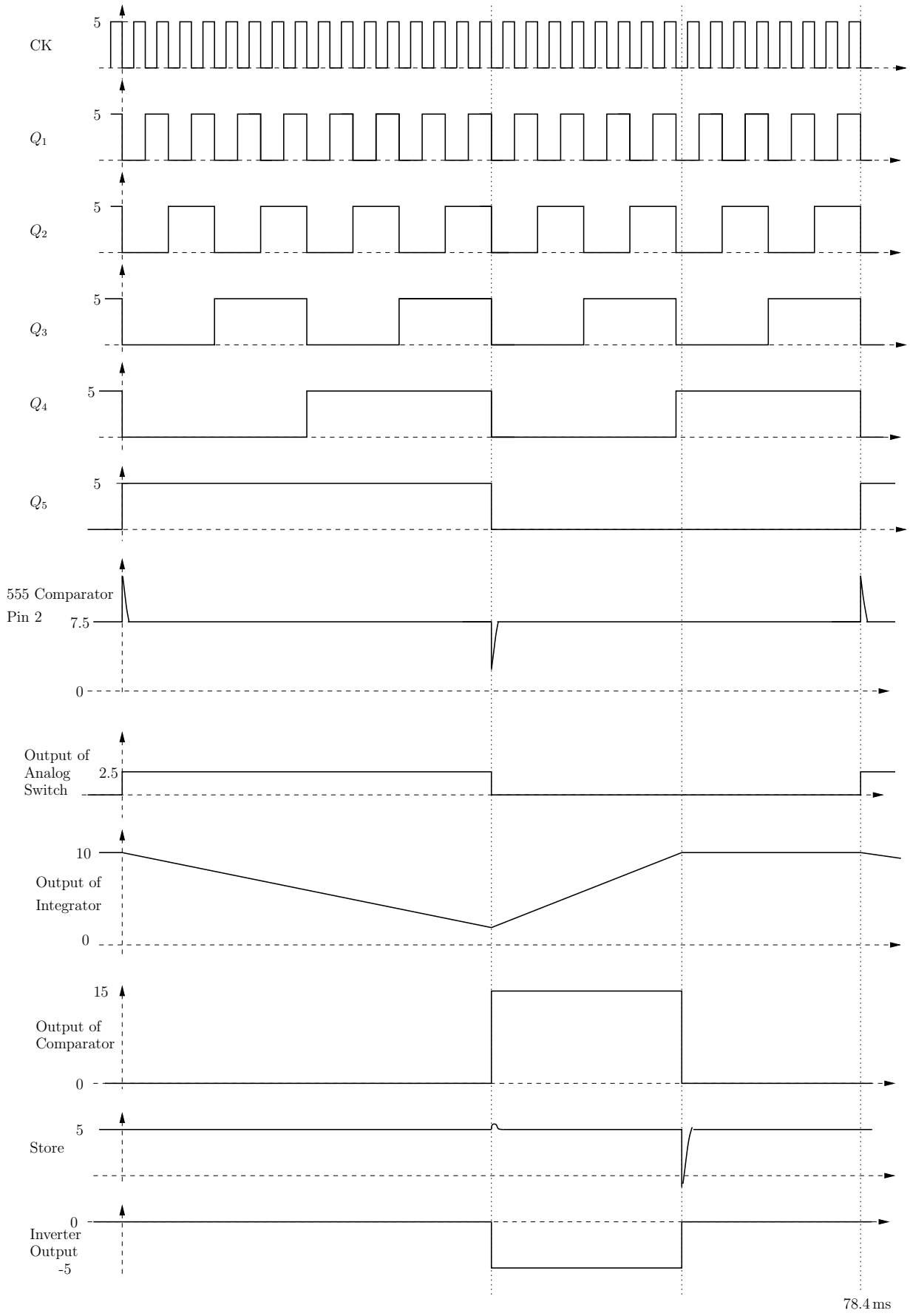
103. In lab you built a dual-slope analog-to-digital converter, and you completed a timing diagram for important signals. The following page gives a timing diagram that I made from my version of the A/D converter when I had an input voltage of 2.5 V.

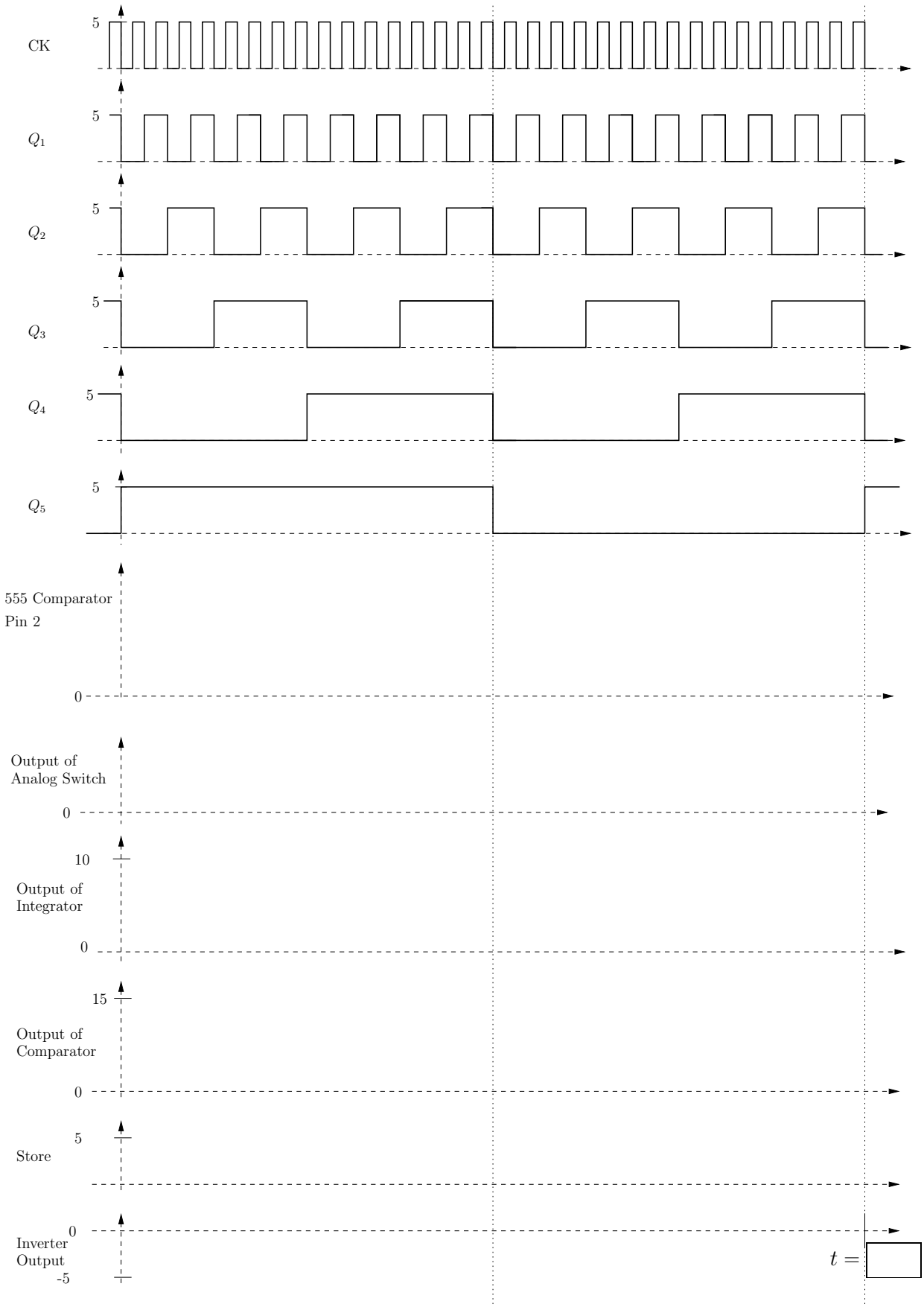
(a) What is the binary output of my A/D converter for the input voltage of 2.5 V? (This should be clear from the timing diagram.)

(b) Redraw the timing diagram for the case in which the input voltage is 1.25 V (rather than 2.5 V. What is the binary output? (A blank timing diagram is on the page following my timing diagram; print copies as needed for this and the following questions.)

(c) Now imagine returning to an input voltage of 2.5 V, but this time add an additional 0.1 μF capacitor in parallel with the capacitor in the clock. Redraw the timing diagram. What is the binary output?

(d) Imagine returning to the original capacitance in the clock, but this time add an additional 0.1 μF capacitor in parallel with the capacitor in the integrator. Redraw the timing diagram for an input of 2.5 V. What is the binary output?


CK
5
Q_1
5
Q_2
5
Q_3
5
Q_4
5
Q_5
5
555 Comparator
Pin 2
7.5
0
Output of
Analog
Switch
2.5
10
Output of
Integrator
0
15
Output of
Comparator
0
5
Store
0
Inverter
Output
-5
78.4 ms


CK
5
Q_1
5
Q_2
5
Q_3
5
Q_4
5
Q_5
5
555 Comparator
Pin 2
0
Output of
Analog Switch
0
10
Output of
Integrator
0
15
Output of
Comparator
0
5
Store
0
Inverter
Output
-5
$t =$

104. Design a digital to analog converter that will convert a three-bit binary number into an analog voltage with 000_2 corresponding to 0 V and 111_2 corresponding to 1.225 V.

105. Use a computer graphing tool to make graphs of the following sums:

(a)

$$s_a(t) = \sum_{n=1}^{1} \frac{4\left((-1)^{(n+1)} + 1\right)}{(n\pi)^2} \cos(2n\pi t).$$

(b)

$$s_b(t) = \sum_{n=1}^{3} \frac{4\left((-1)^{(n+1)} + 1\right)}{(n\pi)^2} \cos(2n\pi t).$$

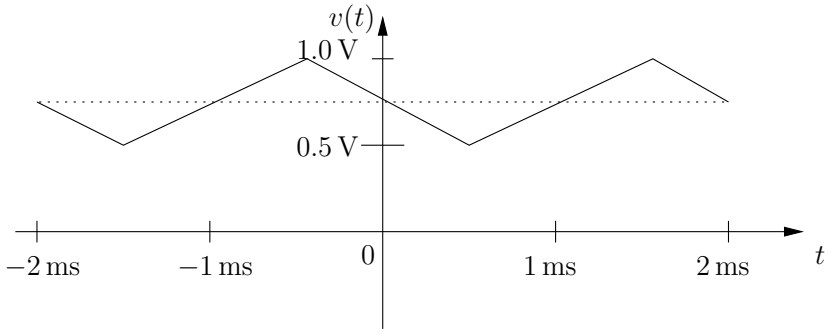
(c)

$$s_c(t) = \sum_{n=1}^{5} \frac{4\left((-1)^{(n+1)} + 1\right)}{(n\pi)^2} \cos(2n\pi t).$$

(d)

$$s_d(t) = \sum_{n=1}^{101} \frac{4\left((-1)^{(n+1)} + 1\right)}{(n\pi)^2} \cos(2n\pi t).$$

106. Consider the following graph of a periodic voltage signal:



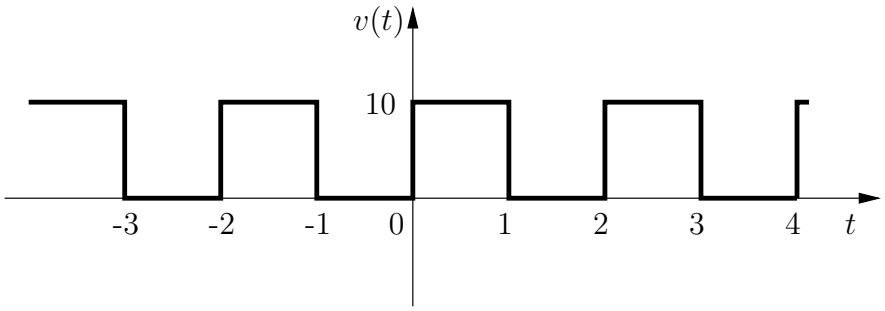
All (well-behaved) periodic signals can be represented by a Fourier series:

$$v(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos n\omega t + \sum_{m=1}^{\infty} b_m \sin m\omega t.$$

From the graph, estimate the following quantities: ω_1, a_0, a_1, b_1, and a_2. What is the sign of b_2?

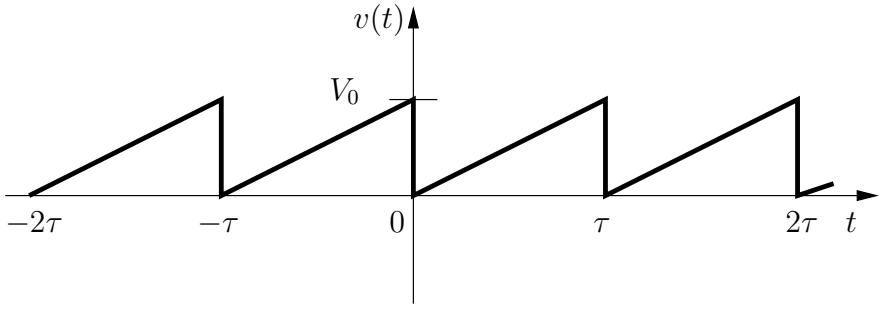
107. Fourier analyze the illustrated periodic square wave, i.e., determine values for the coefficients a_0, a_n, and b_n, and for ω, in the Fourier representation of the signal,

$$v(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos n\omega t + \sum_{m=1}^{\infty} b_m \sin m\omega t.$$



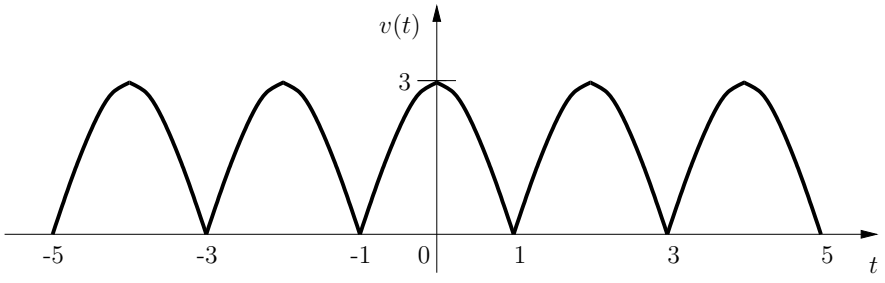
108. Fourier analyze the illustrated periodic sawtooth wave, i.e., determine expressions for the coefficients a_0, a_n, and b_n, and for ω, in the Fourier representation of the signal,

$$v(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos n\omega t + \sum_{m=1}^{\infty} b_m \sin m\omega t.$$



109. Fourier analyze the illustrated periodic signal, which is a sequence of positive half-sine waves, i.e., determine values for the coefficients a_0, a_n, and b_n, and for ω, in the Fourier representation of the signal,

$$v(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos n\omega t + \sum_{m=1}^{\infty} b_m \sin m\omega t.$$



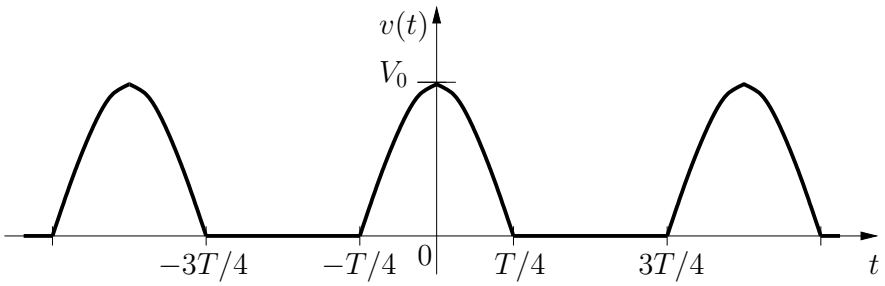
110. Fourier analyze the illustrated periodic rectified sine wave, i.e., determine expressions for the coefficients a_0, a_n, and b_n, and for ω, in the Fourier representation of the signal,

$$v(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos n\omega t + \sum_{m=1}^{\infty} b_m \sin m\omega t.$$

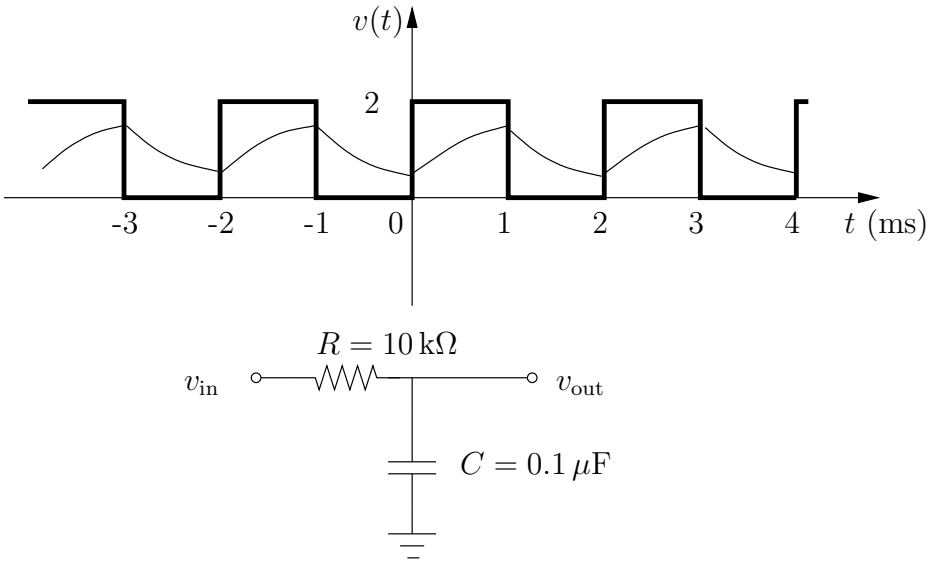
You should find that $b_m = 0$ for all values of m, and

$$a_n = \frac{2V_0}{\pi(1-n^2)} \cos\left(\frac{n\pi}{2}\right)$$

(or some equivalent expression). From this you should show that $a_0 = 2V_0/\pi$, $a_1 = V_0/2$, $a_2 = 2V_0/(3\pi)$, $a_4 = -2V_0/(15\pi)$, and for all odd values of $n > 1$, $a_n = 0$.



111. In lab you observed the output of a low-pass RC low-pass filter when the input was a square wave; the output of a 500 Hz square wave for the given filter looked something like that illustrated in the figure below. (Note that the time axis units are milliseconds.)



In this problem you will construct the output v_{out} in three steps. You will

- Fourier analyze the square wave in order to write it as a sum of sinusoidal terms (you may use previous results for similar square waves)

$$v_{\text{in}}(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos n\omega t + \sum_{m=1}^{\infty} b_m \sin m\omega t.$$

- modify each term in the Fourier decomposition according to the known action of a low-pass filter on a sinusoidal input ($a_n \to a'_n$, $b_n \to b'_n$, add appropriate phase shifts); and
- recombine the modified sinusoidal terms in a new sum.

$$v_{\text{out}}(t) = \frac{a'_0}{2} + \sum_{n=1}^{\infty} a'_n \cos(n\omega t + \phi_n) + \sum_{m=1}^{\infty} b'_m \sin(m\omega t + \phi_m).$$

Complete the table below, and make graphs of your Fourier series approximation of v_{out} using 1, 2, 3, and "many" non-zero terms in your series.

$n\ (m)$	a_n	b_m	a'_n	b'_m	ϕ
0		XXX		XXX	XXX
1					
2					
3					
formula					